

EXHIBIT A – Plaintiff’s Terms and Supporting Evidence**I. “transceiver” – PATENT FAMILIES 1, 2, 3, 6, AND 9.**

<u>No.</u>	<u>Term</u>	<u>Asserted Claims</u> <u>(Families 1, 2, 3, 6, and 9)</u>	<u>Plaintiff’s Construction and Supporting Evidence</u>
1.	<p>“transceiver”</p> <p><u>Family 1:</u> ’686 Patent: Claims 17, 36, 40</p> <p><u>Family 2:</u> ’881 Patent: Claims 17, 18, 21, 23, 25, 26, 29, 31, 33, and 37</p> <p>’193 Patent: Claims 1, 9, 10, 11, 12, 13</p> <p>’601 Patent: Claims 8, 9, 13, 14, 15, 16, 17, 18, 21</p> <p>’014 Patent: Claims 1, 3</p> <p><u>Family 3:</u> ’882 Patent: Claims 9, 13</p> <p>’048 Patent: Claims 1, 5</p> <p>’5473 Patent: Claims 10, 28</p>	<p><u>’686 Patent (Family 1)</u></p> <p>17. An information storage media comprising instructions that when executed communicate diagnostic information over a communication channel using multicarrier modulation comprising:</p> <p>instructions that when executed direct a transceiver to receive or transmit an initiate diagnostic mode message; and</p> <p>instructions that when executed transmit a diagnostic message from the transceiver using multicarrier modulation, wherein the diagnostic message comprises a plurality of data variables representing the diagnostic information about the communication channel and each bit in the diagnostic message is mapped to at least one DMT symbol, and wherein one variable comprises an array representing frequency domain received idle channel noise information.</p> <p>36. An information storage media comprising instructions that when executed communicate diagnostic information over a communication channel using multicarrier modulation comprising:</p>	<p>Plain and ordinary meaning, which is: “communications device capable of transmitting and receiving data wherein the transmitter portion and receiver portion share at least some common circuitry.”</p> <p>’686 Patent: Fig. 1, Cols. 1:54-2:11, 5:11-32.</p> <p>1998 & 2004 MerriamWebster Dictionary definition of “transceiver”: a radio transmitter-receiver that uses many of the same components for both transmission and reception.</p> <p>2002 McGraw-Hill Dictionary of Scientific and Technical Terms definition of “transceiver”: A radio transmitter and receiver combined in one unit and having switching arrangements such as to permit both transmitting and receiving.</p>

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	<p>’608 Patent: Claims 1, 2, 3, 4</p> <p>’510 Patent: Claims 21, 22</p> <p><u>Family 6:</u></p> <p>’835 Patent: Claims 8, 24</p> <p>’112 Patent: Claims 8, 10, 11, 12, 14</p> <p><u>Family 9:</u></p> <p>’411 Patent: Claims 10, 11, 17, 18, 19, 25</p> <p>’577 Patent: Claims 16, 17, 30, 31, 37, 38, 53, 54</p> <p>’348 Patent: Claims 1, 3, 9, 11</p> <p>’055 Patent: Claims 11, 17, 19</p> <p>’4473 Patent: Claims 1, 3</p> <p>’809 Patent: Claims 1, 3, 4, 6, 8, 10, 11, 13, 15, 17, 18, 20, 22, 24, 25, 27</p>	<p>instructions that when executed direct a transceiver to receive or transmit an initiate diagnostic mode message; and</p> <p>instructions that when executed transmit from the transceiver a diagnostic message using multicarrier modulation with DMT symbols that are mapped to one bit of the diagnostic message, wherein the diagnostic message comprises a plurality of data variables representing the diagnostic information about the communication channel, and wherein one variable comprises an array representing is frequency domain received idle channel noise information.</p> <p>40. In a multicarrier modulation transceiver, a method of communicating diagnostic information over a communication channel using multicarrier modulation comprising:</p> <p>transmitting, during a diagnostic mode, a diagnostic message using multicarrier modulation, wherein the diagnostic message comprises a plurality of data variables representing the diagnostic information about the communication channel and at least one bit in the diagnostic message is mapped to at least one DMT symbol, wherein one variable comprises an array</p>	

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		<p>representing frequency domain received idle channel noise information.</p> <p><u>’881 Patent (Family 2)</u></p> <p>17. A plurality of bonded transceivers, each bonded transceiver utilizing at least one transmission parameter value to reduce a difference in latency between the bonded transceivers, wherein a data rate for a first of the bonded transceivers is different than a data rate for a second of the bonded transceivers.</p> <p>18. The transceivers of claim 17, wherein the at least one transmission parameter value is a Reed Solomon Coding parameter value, an interleaving parameter value, a coding parameter value, a codeword size value or a framing parameter value.</p> <p>21. The transceiver of claim 17, wherein the at least one transmission parameter value for the first transceiver is a first Reed Solomon Coding parameter value that is different than a second Reed Solomon Coding parameter value for the second transceiver.</p> <p>23. The transceivers of claim 17, wherein the at least one transmission parameter value for the first transceiver is a first interleaving parameter value that is different than a second</p>	

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		<p>interleaving parameter value for the second transceiver.</p> <p>25. A plurality of bonded transceivers, each bonded transceiver selecting at least one transmission parameter value to reduce a difference in latency between the bonded transceivers, wherein a data rate for a first of the bonded transceivers is different than a data rate for a second of the bonded transceivers.</p> <p>26. The transceivers of claim 25, wherein the at least one transmission parameter value is a Reed Solomon Coding parameter value, an interleaving parameter value, a coding parameter value, a codeword size value or a framing parameter value.</p> <p>29. The transceivers of claim 25, wherein the at least one transmission parameter value for the first transceiver is a first Reed Solomon Coding parameter value that is different than a second Reed Solomon Coding parameter value for the second transceiver.</p> <p>31. The transceivers of claim 25, wherein the at least one transmission parameter value for the first transceiver is a first interleaving parameter value that is different than a second interleaving parameter value for the second</p>	

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		<p>transceiver parameter value when the data rate for the first transceiver is less than the data rate for the second transceiver.</p> <p>33. A storage media having computer executable instructions stored thereon that: utilize at least one transmission parameter value, for each transceiver in a plurality of bonded transceivers, to reduce a difference in latency between the bonded transceivers, wherein a data rate for a first of the plurality of bonded transceivers is different than a data rate for a second of the plurality of bonded transceivers.</p> <p>37. A storage media having computer executable instructions stored thereon that: select at least one transmission parameter value, for each transceiver in a plurality of bonded transceivers, to reduce a difference in latency between the bonded transceivers, wherein a data rate of a first of the plurality of bonded transceivers is different than a data rate of a second of the plurality of bonded transceivers.</p> <p><u>’193 Patent (Family 2)</u></p> <p>1. A device comprising:</p>	

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		<p>a plurality of transceivers configurable to simultaneously operate with a combination of bonded and unbonded transceivers, wherein a first transceiver of the plurality of transceivers is operable at a first data rate, and a second transceiver of the plurality of transceivers is simultaneously operable at a second data rate that is different than the first data rate, wherein the first and second transceivers are operable as bonded transceivers and wherein a third transceiver, of the plurality of transceivers, is simultaneously operable at a third data rate and the third transceiver is not bonded with any other transceiver.</p> <p>9. A device comprising: a plurality of transceivers configurable to simultaneously operate with a combination of bonded and unbonded transceivers, wherein a first transceiver of the plurality of transceivers transmits at a first data rate, and a second transceiver of the plurality of transceivers simultaneously transmits at a second data rate that is different than the first data rate, wherein the first and second transceivers operate as bonded transceivers and wherein a third transceiver, of the plurality of transceivers,</p>	

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		<p>simultaneously transmits at a third data rate and the third transceiver is not bonded with any other transceiver.</p> <p>10. The device of claim 9, wherein the transceivers are capable of transmitting cells or ATM cells.</p> <p>11. The device of claim 9, wherein the transceivers are capable of transmitting packets, Ethernet packets or Internet Protocol packets.</p> <p>12. The device of claim 9, wherein the first and second transceivers generate a single high data rate connection between a service provider and a subscriber.</p> <p>13. The device of claim 9, wherein first and the second transceivers are operable to utilize at least one parameter associated with operation of at least one of the first and second transceivers to reduce a difference in latency between the first and second transceivers.</p> <p><u>’601 Patent (Family 2)</u></p> <p>8. A device comprising: a plurality of transceivers, wherein a first transceiver of the plurality of transceivers</p>	

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		<p>is operable to transmit at a first data rate on a first twisted-pair line, and</p> <p>a second transceiver of the plurality of transceivers is simultaneously operable to transmit at a second data rate on a second twisted-pair line, wherein the first data rate and the second data rate are capable of being different and wherein the first and second twisted-pair lines are capable of providing DSL service to a first subscriber, and</p> <p>wherein a third transceiver, of the plurality of transceivers, is simultaneously operable to transmit at a third data rate on a third twisted-pair line, wherein the third twisted-pair line is capable of providing DSL service to a second subscriber, wherein the first and second transceivers are connected to a multi-pair multiplexer.</p> <p>9. The device claim 8, wherein the first, second and third of transceivers are connected to a virtual path/virtual channel multiplexer and the third transceiver is not connected to the multi-pair multiplexer.</p>	

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		<p>13. The device of claim 8, wherein the first and second transceivers are capable of generating a single high data rate connection between a service provider and a subscriber.</p> <p>14. The device of claim 8, wherein the first and the second transceivers are operable to utilize at least one parameter associated with operation of at least one of the first and second transceivers to reduce a difference in latency between the first and second transceivers.</p> <p>15. A device comprising: a multi-pair multiplexer, and a plurality of transceivers, including: a first transceiver, a second transceiver, and a third transceiver, the device capable of bonding at least the first and second transceivers of the plurality of transceivers, while at least the third transceiver of the plurality of transceivers is not bonded with any other transceivers in the device, and wherein the at least two bonded transceivers are operable at different data rates, and wherein the first and second transceivers are connected to multi-pair multiplexer and the third</p>	

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		<p>transceiver is not connected to the multi-pair multiplexer.</p> <p>16. The device of claim 15, wherein the plurality of transceivers are connected to a virtual path/virtual channel multiplexer.</p> <p>17. The device of claim 15, wherein the transceivers are capable of transmitting cells or ATM cells.</p> <p>18. The device of claim 15, wherein the transceivers are capable of transmitting packets, Ethernet packets or Internet Protocol packets.</p> <p>21. The device of claim 15, wherein the at least two transceivers are operable to utilize at least one parameter associated with operation of at least one of the first and second transceivers to reduce a difference in latency between the first and second transceivers.</p> <p><u>’014 Patent (Family 2)</u></p> <p>1. A device comprising: plurality of transceivers configurable to simultaneously operate with a combination of bonded and unbonded transceivers, wherein a first transceiver of the plurality</p>	

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		<p>of transceivers is operable at a first data rate, and a second transceiver of the plurality of transceivers is simultaneously operable at a second data rate that is different than the first data rate, wherein the first and second transceivers are operable as bonded transceivers, and wherein a third transceiver, of the plurality of transceivers, is simultaneously operable at a third data rate, different than the first data rate and the second data rate, and the third transceiver is not bonded with any other transceiver,</p> <p>wherein the first and second transceivers are VDSL transceivers that are operable to transmit Internet Protocol (IP) packets, and wherein the third transceiver is a ADSL transceiver operable to transmit ATM cells.</p> <p>3. The device of claim 1, wherein the first and second transceivers generate a single high data rate connection between a service provider and a subscriber.</p> <p><u>’882 Patent (Family 3)</u></p> <p>9. A system that allocates shared memory comprising: a transceiver that performs:</p>	

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		<p>transmitting or receiving a message during initialization specifying a maximum number of bytes of memory that are available to be allocated to an interleaver, determining an amount of memory required by the interleaver to interleave a first plurality of Reed Solomon (RS) coded data bytes within a shared memory; allocating a first number of bytes of the shared memory to the interleaver to interleave the first plurality of Reed Solomon (RS) coded data bytes for transmission at a first data rate, wherein the allocated memory for the interleaver does not exceed the maximum number of bytes specified in the message; allocating a second number of bytes of the shared memory to a deinterleaver to deinterleave a second plurality of RS coded data bytes received at a second data rate; and interleaving the first plurality of RS coded data bytes within the shared memory allocated to the interleaver and deinterleaving the second plurality of RS coded data bytes within the shared memory allocated to the deinterleaver, wherein the shared memory allocated to the interleaver is used at the same time as the</p>	

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		<p>shared memory allocated to the deinter-leaver.</p> <p>13. A system that allocates shared memory comprising:</p> <p>a transceiver that performs:</p> <p>transmitting or receiving a message during initialization specifying a maximum number of bytes of memory that are available to be allocated to a deinter-leaver;</p> <p>determining an amount of memory required by the deinterleaver to deinterleave a first plurality of Reed Solomon (RS) coded data bytes within a shared memory;</p> <p>allocating a first number of bytes of the shared memory to the deinterleaver to deinterleave a first plurality of Reed Solomon (RS) coded databytes for transmission at a first data rate, wherein the allocated memory for the deinterleaver does not exceed the maximum number of bytes specified in the message;</p> <p>allocating a second number of bytes of the shared memory to an interleaver to interleave a second plurality of RS coded data bytes received at a second data rate;</p> <p>and</p> <p>deinterleaving the first plurality of RS coded data bytes within the shared</p>	

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		<p>memory allocated to the deinterleaver and interleaving the second plurality of RS coded data bytes within the sh[a]red memory allocated to the interleaver, wherein the shared memory allocated to the deinterleaver is used at the same time as the shared memory allocated to the in - terleaver.</p> <p><u>’048 Patent (Family 3)</u></p> <p>1. A system that allocates shared memory comprising:</p> <p>a transceiver that is capable of transmitting or receiving a message during initialization specifying a maximum number of bytes of memory that are available to be allocated to an interleaver;</p> <p>determining an amount of memory required by the interleaver to interleave a first plurality of Reed Solomon (RS) coded data bytes within the shared memory;</p> <p>allocating a first number of bytes of the shared memory to the interleaver to in - terleave the first plurality of Reed Solomon (RS) coded data bytes for transmission at a first data rate, wherein the allocated memory for the interleaver does not exceed the maximum number of bytes specified in the message;</p>	

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		<p>allocating a second number of bytes of the shared memory to a deinterleaver to deinterleave a second plurality of RS coded data bytes received at a second data rate; and</p> <p>interleaving the first plurality of RS coded data bytes within the shared memory allocated to the interleaver and deinterleaving the second plurality of RS coded data bytes within the shared memory allocated to the deinterleaver, wherein the shared memory allocated to the interleaver is used at the same time as the shared memory allocated to the deinterleaver.</p> <p>5. A system that allocates shared memory comprising: a transceiver that is capable of: transmitting or receiving a message during initialization specifying a maximum number of bytes of memory that are available to be allocated to a deinterleaver; determining an amount of memory required by the deinterleaver to deinterleave a first plurality of Reed Solomon (RS) coded data bytes within the shared memory;</p>	

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		<p>allocating a first number of bytes of the shared memory to the deinterleaver to deinterleave a first plurality of ReedSolomon (RS) coded data bytes for transmission at a first data rate, wherein the allocated memory for the deinterleaver does not exceed the maximum number of bytes specified in the message;</p> <p>allocating a second number of bytes of the shared memory to an interleaver to interleave a second plurality of RS coded data bytes received at a second data rate;</p> <p>and</p> <p>deinterleaving the first plurality of RS coded data bytes within the shared memory allocated to the deinterleaver and interleaving the second plurality of RS coded data bytes within the shared memory allocated to the interleaver, wherein the shared memory allocated to the deinterleaver is used at the same time as the shared memory allocated to the interleaver.</p> <p><u>’5473 Patent (Family 3)</u></p> <p>10. A multicarrier communications transceiver with a shared memory, the transceiver capable of:</p> <p>sharing the memory between an interleaver in a first latency path and</p>	

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		<p>a deinterleaver in a second latency path; and transmitting or receiving, during initializa - tion of the transceiver, a message indicat - ing how the shared memory is to be used by the interleaver or the deinterleaver.</p> <p><u>’608 Patent (Family 3)</u></p> <p>1. A transceiver comprising:</p> <p>a transmitter portion operable to transmit a first message over a channel, wherein the first message indicates a first maximum number of bytes associated with an inter leaver function of a transmit latency path and a first maximum number of bytes asso - ciated with a deinterleaver function of a re - ceive latency path; and</p> <p>a receiver portion operable to determine a change in a channel condition for the chan - nel;</p> <p>the transmitter portion further operable to transmit a second message over the channel after determining the change in the channel condition, wherein the second message in - dicates a second maximum number of bytes associated with the interleaver func - tion of the transmit latency path and a sec - ond maximum number of bytes associated with the deinterleaver function of the re - ceive latency path,</p>	

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		<p>wherein the first maximum number of bytes associated with the interleaver function of the transmit latency path is different than the second maximum number of bytes as sociated with the interleaver function of the transmit latency path, and</p> <p>wherein the first maximum number of bytes associated with the deinterleaver function of the receive latency path is different than the second maximum number of bytes as sociated with the deinterleaver function of the receive latency path.</p> <p>2. The transceiver of claim 1, further comprising a memory wherein the memory is operable to be shared between the interleaver function of the transmitter portion associated with the transmit latency path and the deinterleaver function of the receiver portion associated with the receive latency path, wherein the first maximum number of bytes associated with the interleaver function is used to determine how much memory is used by the interleaver function and wherein the first maximum number of bytes associated with the deinterleaver function is used to determine how much memory is used by the deinterleaver function, wherein the sharing comprises using a first portion of the memory for the interleaver</p>	

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		<p>function and simultaneously using a second portion of the memory, different than the first portion, for the deinterleaver function, and the first and second portions of the memory are configurable such that one or more bytes of the memory can be used by the interleaver function at one particular time and the same one or more bytes of the memory can be used by the deinterleaver function at a second time, different than the first time.</p> <p>3. The transceiver of claim 2, wherein the second maximum number of bytes associated with the interleaver function of the transmit latency path is used to determine how much memory is used by the interleaver function, and wherein the second maximum number of bytes associated with the deinterleaver function of the receive latency path is used to determine how much memory used by the deinterleaver function.</p> <p>4. A transceiver comprising: a transmitter portion operable to transmit a first message over a channel at a first time, wherein the first message indicates a first maximum number of bytes associated with an interleaver function of a transmit latency</p>	

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		<p>path and a first maximum number of bytes associated with a deinterleaver function of a receive latency path; and</p> <p>a receiver portion operable to determine a change in a channel condition of the channel,</p> <p>wherein the transmitter portion is further operable to transmit a second message over the channel at a second time after determining the change in the channel condition, wherein the second message indicates a second maximum number of bytes associated with the interleaver function of the transmit latency path and a second maximum number of bytes associated with the deinterleaver function of the receive latency path,</p> <p>wherein the first maximum number of bytes associated with the interleaver function of the transmit latency path is different than the second maximum number of bytes associated with the interleaver function of the transmit latency path,</p> <p>wherein the first maximum number of bytes associated with the deinterleaver function of the receive latency path is different than the second maximum number of bytes associated with the deinterleaver function of the receive latency path,</p>	

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		<p>wherein the first time is different than the second time, and</p> <p>wherein one or more bytes of memory is used by the interleaver function of the transmitter portion at the first time and the same one or more bytes of the memory are used by the deinterleaver function of the receiver portion at the second time.</p> <p><u>’510 Patent (Family 3)</u></p> <p>21. A device comprising:</p> <p>a transceiver operable to allocate a first portion of shared memory to an interleaver in a transmit latency path and operable allocate a second portion of the shared memory to a deinterleaver in a receiver latency path;</p> <p>the transceiver further operable to transmit to another transceiver information that indicates the shared memory allocation between the interleaver and the deinterleaver, and</p> <p>and operable to update the shared memory allocation between the interleaver and deinterleaver based on changing communication conditions, wherein the changing communications conditions include a change in channel conditions.</p>	

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		<p>22. The device of claim 21, wherein the transceiver is further operable to transmit to another transceiver information that indicates the updated shared memory allocation between the interleaver and the deinterleaver.</p> <p><u>’835 Patent (Family 6)</u></p> <p>8. An apparatus configurable to adapt forward error correction and interleaver parameter (FIP) settings during steady-state communication or initialization comprising:</p> <p>a transceiver, including a processor, configurable to: transmit a signal using a first FIP setting, transmit a flag signal, and switch to using for transmission, a second FIP setting following transmission of the flag signal,</p> <p>wherein:</p> <p>the first FIP setting comprises at least one first FIP value, the second FIP setting comprises at least one second FIP value, different than the first FIP value, and the switching occurs on a pre-defined forward error correction codeword boundary following the flag signal.</p>	

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		<p>24. An apparatus configurable to adapt forward error correction and interleaver parameter (FIP) settings during steady-state communication or initialization comprising: a transceiver, including a processor, configurable to: receive a signal using a first FIP setting, receive a flag signal, and Switch to using for reception, a second FIP setting following reception of the flag signal, wherein: the first FIP setting comprises at least one first FIP value, the second FIP setting comprises at least one second FIP value, different than the first FIP value, and the switching occurs on a pre-defined forward error correction codeword boundary following the flag signal.</p> <p><u>’112 Patent (Family 6)</u></p> <p>8. A transceiver comprising: a receiver operable to receiving, during steady-state communication, using a first forward error correction and interleaving parameter (FIP) setting that comprises a forward error correction (FEC) codeword size and a first number of FEC coding parity bytes; and the receiver further operable to switch, during the steady state communication, to re-</p>	

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		<p>ceiving using a second FIP setting that comprises a second FEC codeword size that is different than the first FEC code word size and a second number of FEC coding parity bytes that is different than the first number of FEC coding parity bytes,</p> <p>wherein the switching to receiving using the second FEC codeword size and the second number of FEC coding parity bytes is based on a counter reaching a value.</p> <p>10. The transceiver of claim 8, wherein the switching to receiving using the second FEC codeword size and the second number of FEC coding parity bytes does not cause bit errors or service interruption.</p> <p>11. The transceiver of claim 8, wherein the switching to receiving using the second FEC codeword size and the second number of FEC coding parity bytes is associated with at least one of an impulse noise protection value, a data 25 rate and a latency value.</p> <p>12. The transceiver of claim 8, wherein the switching to receiving using the second FEC codeword size and the second number of FEC</p>	

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<u>No.</u>	<u>Term</u>	<u>Asserted Claims</u> <u>(Families 1, 2, 3, 6, and 9)</u>	<u>Plaintiff’s Construction and Supporting Evidence</u>
		<p>coding parity bytes is associated with a service provider configuration.</p> <p>14. The transceiver of claim 8, wherein a data rate and/or latency do not change when switching to receiving using the second FEC codeword size and the second number of FEC coding parity bytes.</p> <p><u>’411 Patent (Family 9)</u></p> <p>10. A transceiver capable of packet retransmission comprising:</p> <p>a transmitter portion capable of transmitting a plurality of packets, identifying at least one packet of the plurality of packets as a packet that should be retransmitted and allocating a memory between a retransmission function and an interleaving and/or deinterleaving function, wherein at least a portion of the memory may be allocated to the retransmission function or to the interleaving and/or deinterleaving function at any one particular time, and wherein a message transmitted during initialization indicates how the memory has been allocated between the retransmission function and the interleaving and/or deinterleaving function in the transceiver.</p>	

EXHIBIT A – Plaintiff’s Terms and Supporting Evidence

<u>No.</u>	<u>Term</u>	<u>Asserted Claims</u> <u>(Families 1, 2, 3, 6, and 9)</u>	<u>Plaintiff’s Construction and Supporting</u> <u>Evidence</u>
		<p>11. The transceiver of claim 10, wherein the packets are used for video applications.</p> <p>17. The transceiver of claim 10, wherein a sum of a maximum amount of the memory that can be allocated to the retransmission function and a maximum amount of the memory that can be allocated to the interleaving/deinterleaving function is more than a total amount of the memory.</p> <p>18. A transceiver capable of packet retransmission comprising: a receiver portion capable of receiving a plurality of packets, identifying at least one packet of the plurality of packets as a packet that should be retransmitted and allocating a memory between a retransmission function and an interleaving and/or deinterleaving function wherein the memory is allocated between the interleaving function and the deinterleaving function in accordance with a message received during an initialization of the transceiver and wherein at least a portion of the memory may be allocated between the retransmission function and the retransmission and/or deinterleaving function at</p>	

EXHIBIT A – Plaintiff’s Terms and Supporting Evidence

<u>No.</u>	<u>Term</u>	<u>Asserted Claims</u> <u>(Families 1, 2, 3, 6, and 9)</u>	<u>Plaintiff’s Construction and Supporting Evidence</u>
		<p>any one particular time depending on the message.</p> <p>19. The transceiver apparatus of claim 18, wherein the packets are used for video applications.</p> <p>25. The transceiver of claim 18, wherein a sum of a maximum amount of the memory that can be allocated to the retransmission function and a maximum amount of the memory that can be allocated to the interleaving and/or de-interleaving function is more than a total amount of the memory.</p> <p><u>’577 Patent (Family 9)</u></p> <p>16. An apparatus comprising: a multicarrier transceiver operable to receive at least one packet using deinterleaving, and transmit at least one message with out using interleaving, wherein the at least one message includes information that indicates an acknowledgement (ACK) or a negative acknowledgement (NACK) of the at least one packet, wherein the at least one packet comprises one or more PTM-TC codewords.</p>	

EXHIBIT A – Plaintiff’s Terms and Supporting Evidence

<u>No.</u>	<u>Term</u>	<u>Asserted Claims</u> <u>(Families 1, 2, 3, 6, and 9)</u>	<u>Plaintiff’s Construction and Supporting Evidence</u>
		<p>17. The apparatus of claim 16, wherein the transceiver is operable to receive at least one retransmitted packet using interleaving.</p> <p>30. An apparatus comprising:</p> <p>a multicarrier transceiver operable to receive at least one packet using deinterleaving, and transmit at least one message without using interleaving, wherein the at least one message includes information that indicates an acknowledgement (ACK) or a negative acknowledgement (NACK) of the at least one packet, wherein the at least one packet comprises one or more Reed-Solomon codewords.</p> <p>31. The apparatus of claim 30, wherein the transceiver is operable to receive at least one retransmitted packet using interleaving.</p> <p>37. An apparatus comprising:</p> <p>a multicarrier transceiver operable to transmit at least one packet using interleaving, and receive at least one message without using interleaving, wherein the at least one message includes information that indicates an acknowledgement (ACK) or a negative acknowledgement (NACK) of the at least one packet, wherein the at least one</p>	

EXHIBIT A – Plaintiff’s Terms and Supporting Evidence

<u>No.</u>	<u>Term</u>	<u>Asserted Claims</u> <u>(Families 1, 2, 3, 6, and 9)</u>	<u>Plaintiff’s Construction and Supporting</u> <u>Evidence</u>
		<p>packet comprises one or more PTM-TC codewords.</p> <p>38. The apparatus of claim 37, wherein the transceiver is operable to retransmit at least one packet using interleaving.</p> <p>53. An apparatus comprising: a multicarrier transceiver operable to transmit at least one packet using interleaving, and receive at least one message without using interleaving, wherein the at least one message includes information that indicates an acknowledgement (ACK) or a negative acknowledgement (NACK) of the at least one packet, wherein the at least one packet comprises one or more Reed-Solomon codewords.</p> <p>54. The apparatus of claim 53, wherein the transceiver is operable to retransmit at least one packet using interleaving.</p> <p><u>’348 Patent (Family 9)</u></p> <p>1. An apparatus comprising: a multicarrier transceiver including a processor and memory operable to: transmit a packet using a forward error correction encoder and an interleaver, wherein the packet comprises a header field and a</p>	

EXHIBIT A – Plaintiff’s Terms and Supporting Evidence

<u>No.</u>	<u>Term</u>	<u>Asserted Claims</u> <u>(Families 1, 2, 3, 6, and 9)</u>	<u>Plaintiff’s Construction and Supporting</u> <u>Evidence</u>
		<p>plurality of PTM-TC codewords, a plurality of ATM cells or a plurality of Reed-Solomon codewords, and wherein the header field comprises a sequence identifier (SID); and</p> <p>receive a plurality of messages using a forward error correction decoder and without using a deinterleaver, wherein each message of the plurality of messages is received in a different DMT symbol and wherein at least one message of the plurality of messages includes an acknowledgment (ACK) or a negative acknowledgment (NACK) of the transmitted packet.</p> <p>3. The apparatus of claim 1, wherein the transceiver is operable to retransmit the packet using the forward error correction encoder and the interleaver.</p> <p>9. An apparatus comprising: a multicarrier transceiver including a processor and memory operable to: receive a packet using a forward error correction decoder and a deinterleaver, wherein the packet comprises a header field and a plurality of PTM-TC codewords, a plurality of ATM cells or a plurality of Reed-Solomon codewords, and wherein the header</p>	

EXHIBIT A – Plaintiff’s Terms and Supporting Evidence

<u>No.</u>	<u>Term</u>	<u>Asserted Claims</u> <u>(Families 1, 2, 3, 6, and 9)</u>	<u>Plaintiff’s Construction and Supporting</u> <u>Evidence</u>
		<p>field comprises a sequence identifier (SID); and transmit a plurality of messages using a forward error correction encoder and without using an interleaver, wherein each message of the plurality of messages is transmitted in a different DMT symbol and wherein at least one message of the plurality of messages includes an acknowledgement (ACK) or a negative acknowledgement (NACK) of the received packet.</p> <p>11. The apparatus of claim 9, wherein the transceiver is operable to receive a retransmitted packet using the forward error correction decoder and the deinterleaver.</p> <p><u>’055 Patent (Family 9)</u></p> <p>11. A transceiver operable to transmit a first type of packet and to transmit a second type of packet, wherein the first type of packet is stored in a retransmission buffer after transmission and the second type of packet is not stored in a retransmission buffer after transmission, and wherein the first and second types of packet comprise a header field that indicates whether a transmitted packet is a first type of packet or a second type of packet, and wherein the header field of the first type of packet com-</p>	

EXHIBIT A – Plaintiff’s Terms and Supporting Evidence

<u>No.</u>	<u>Term</u>	<u>Asserted Claims</u> <u>(Families 1, 2, 3, 6, and 9)</u>	<u>Plaintiff’s Construction and Supporting Evidence</u>
		<p>prises a sequence identifier (SID) that is incremented after the first type of packet is transmitted and the header field of the second type of packet does not comprise the SID of the first type of packet.</p> <p>17. The transceiver of claim 11, wherein the first type of packet comprises one or more PTM-TC (Packet Transfer Mode-Transmission Convergence) codewords.</p> <p>19. The transceiver of claim 11, wherein the first type of packet comprises one or more Reed Solomon codewords.</p> <p><u>’4473 Patent (Family 9)</u></p> <p>1. An apparatus comprising: a multicarrier transceiver including a processor and memory operable to reduce a packet error rate by: transmitting, by the transceiver, a packet using a forward error correction encoder and an interleaver, wherein the packet comprises a header field and a plurality of bytes, and wherein the header field comprises a sequence identifier (SID); and receiving, by the transceiver, at least one message using a forward error correction decoder and without using a deinterleaver, wherein the at least one message is received</p>	

EXHIBIT A – Plaintiff’s Terms and Supporting Evidence

<u>No.</u>	<u>Term</u>	<u>Asserted Claims</u> <u>(Families 1, 2, 3, 6, and 9)</u>	<u>Plaintiff’s Construction and Supporting</u> <u>Evidence</u>
		<p>in a single discrete multitone (DMT) symbol and wherein the at least one message includes an acknowledgement (ACK) or a negative acknowledgement (NACK) of the transmitted packet,</p> <p>wherein an SNR margin of the at least one message is greater than an SNR margin of the packet; and</p> <p>reducing the packet error rate by retransmitting, by the transceiver and when there is the negative acknowledgement (NACK) in the at least one message, the packet.</p> <p>3. The apparatus of claim 1, wherein the transceiver is operable to retransmit the packet using the forward error correction encoder and the interleaver.</p> <p><u>’809 Patent (Family 9)</u></p> <p>1. An apparatus comprising: a multicarrier transceiver including a processor and memory capable of: transmitting a packet using forward error correction encoding and interleaving, wherein the packet comprises a header field and a plurality of Reed-Solomon codewords, and wherein the header field comprises a sequence identifier (SID); and receiving a message using forward error correction decoding and without using de-</p>	

EXHIBIT A – Plaintiff’s Terms and Supporting Evidence

<u>No.</u>	<u>Term</u>	<u>Asserted Claims</u> <u>(Families 1, 2, 3, 6, and 9)</u>	<u>Plaintiff’s Construction and Supporting Evidence</u>
		<p>interleaving, wherein the message is received in a single DMT symbol, and wherein the message includes an acknowledgement (ACK) or a negative acknowledgement (NACK) of the transmitted packet.</p> <p>3. The apparatus of claim 1, wherein the transceiver is capable of retransmitting the packet using forward error correction encoding and interleaving.</p> <p>4. The apparatus of claim 1, wherein a physical layer of the transceiver is capable of generating the packet and the message.</p> <p>6. The apparatus of claim 2, wherein a physical layer of the transceiver is capable of generating the packet and the message.</p> <p>8. An apparatus comprising: a multicarrier transceiver including a processor and memory capable of: receiving a packet using forward error correction decoding and deinterleaving, wherein the packet comprises a header field and a plurality of Reed - Solomon code words, and wherein the header field comprises a sequence identifier (SID); and transmitting a message using forward error</p>	

EXHIBIT A – Plaintiff’s Terms and Supporting Evidence

<u>No.</u>	<u>Term</u>	<u>Asserted Claims</u> <u>(Families 1, 2, 3, 6, and 9)</u>	<u>Plaintiff’s Construction and Supporting</u> <u>Evidence</u>
		<p>correction encoding and without using in - interleaving, wherein the message is transmitted in a single DMT symbol and</p> <p>wherein the message includes an acknowledgement (ACK) or a negative acknowledgement (NACK) of the received packet.</p> <p>10. The apparatus of claim 8, wherein the transceiver is capable of receiving a retransmitted packet using forward error correction decoding and deinterleaving.</p> <p>11. The apparatus of claim 8, wherein a physical layer of the transceiver is capable of generating the packet and the message.</p> <p>13. The apparatus of claim 9, wherein a physical layer of the transceiver is capable of generating the packet and the message.</p> <p>15. A non-transitory computer-readable information storage media having stored thereon instructions, that when executed by one or more processors in a transceiver, cause the transceiver to:</p> <p>transmit a packet using forward error correction encoding and interleaving, wherein the packet comprises a header field and a plurality of Reed- Solomon code words, and</p>	

EXHIBIT A – Plaintiff’s Terms and Supporting Evidence

<u>No.</u>	<u>Term</u>	<u>Asserted Claims</u> <u>(Families 1, 2, 3, 6, and 9)</u>	<u>Plaintiff’s Construction and Supporting Evidence</u>
		<p>wherein the header field comprises a sequence identifier (SID); and receive a message using forward error correction decoding and without using deinterleaving, wherein the message is received in a single DMT symbol, and wherein the message includes an acknowledgement (ACK) or a negative acknowledgement (NACK) of the transmitted packet.</p> <p>17. The media of claim 15, wherein instructions further cause the transceiver to retransmit the packet using forward error correction encoding and interleaving.</p> <p>18. The media of claim 15, wherein instructions further cause a physical layer of the transceiver to generate the packet and the message.</p> <p>20. The media of claim 16, wherein instructions further cause a physical layer of the transceiver to generate the packet and the message.</p> <p>22. A non-transitory computer-storage information storage having stored thereon instruc-</p>	

EXHIBIT A – Plaintiff’s Terms and Supporting Evidence

<u>No.</u>	<u>Term</u>	<u>Asserted Claims</u> <u>(Families 1, 2, 3, 6, and 9)</u>	<u>Plaintiff’s Construction and Supporting Evidence</u>
		<p>tions, that, when executed by one or more processors in a transceiver, cause the transceiver to:</p> <p>receive a packet using forward error correction decoding and deinterleaving, wherein the packet comprises a header field and a plurality of Reed - Solomon code words, and wherein the header field comprises a sequence identifier (SID) ; and</p> <p>transmit a message using forward error correction encoding and without using interleaving, wherein the message is transmitted in a single DMT symbol and wherein the message includes an acknowledgment (ACK) or a negative acknowledgment (NACK) of the received packet.</p> <p>24. The media of claim 22, wherein the instructions further cause the transceiver to retransmit the packet using forward error correction decoding and deinterleaving.</p> <p>25. The media of claim 22, wherein instructions further cause a physical layer of the transceiver to generate the packet and the message.</p> <p>27. The media of claim 23, wherein instructions further cause a physical layer of the</p>	

EXHIBIT A – Plaintiff’s Terms and Supporting Evidence

<u>No.</u>	<u>Term</u>	<u>Asserted Claims</u> <u>(Families 1, 2, 3, 6, and 9)</u>	<u>Plaintiff’s Construction and Supporting</u> <u>Evidence</u>
		transceiver to generate the packet and the message.	

EXHIBIT A – Plaintiff’s Terms and Supporting Evidence

II. “operable to” / “configurable to” – PATENT FAMILIES 2, 3, 6, 9, AND 10

<u>No.</u>	<u>Term</u>	<u>Asserted Claims</u> <u>(Families 2, 3, 6, 9, and 10)</u>	<u>Plaintiff’s Construction and Supporting Evidence</u>
2.	<p>“configurable to” / “operable” / “operable to”</p> <p><u>Family 2:</u> ’193 Patent: Claim 1, 9, 13 ’601 Patent: Claims 8, 14, 21 ’014 Patent: Claim 1</p> <p><u>Family 3:</u> ’608 Patent: Claims 1, 4 ’510 Patent: Claim 21, 22</p> <p><u>Family 6:</u> ’112 Patent: Claim 8</p> <p><u>Family 9:</u> ’577 Patent: Claims 16, 17, 30, 31, 37, 38, 53, 54 ’348 Patent: Claims 1, 3, 9, 11 ’055 Patent: Claim 11 ’4473 Patent: Claims 1, 3</p> <p><u>Family 10:</u></p>	<p><u>’193 Patent (Family 2)</u></p> <p>1. A device comprising: a plurality of transceivers configurable to simultaneously operate with a combination of bonded and unbonded transceivers, wherein a first transceiver of the plurality of transceivers is operable at a first data rate, and a second transceiver of the plurality of transceivers is simultaneously operable at a second data rate that is different than the first data rate, wherein the first and second transceivers are operable as bonded transceivers and wherein a third transceiver, of the plurality of transceivers, is simultaneously operable at a third data rate and the third transceiver is not bonded with any other transceiver.</p> <p>9. A device comprising: a plurality of transceivers configurable to simultaneously operate with a combination of bonded and unbonded transceivers, wherein a first transceiver of the plurality of transceivers transmits at a first data rate, and a second transceiver of the plurality of transceivers simultaneously transmits at a second data rate that is differ-</p>	<p>Plain and ordinary meaning, which is: “able to be configured” / “capable” / “capable to”</p>

EXHIBIT A – Plaintiff’s Terms and Supporting Evidence

<u>No.</u>	<u>Term</u>	<u>Asserted Claims</u> <u>(Families 2, 3, 6, 9, and 10)</u>	<u>Plaintiff’s Construction and Supporting Evidence</u>
	<p>’354 Patent: Claim 10</p> <p>’988 Patent: Claim 16</p>	<p>ent than the first data rate, wherein the first and second transceivers operate as bonded transceivers and wherein a third transceiver, of the plurality of transceivers, simultaneously transmits at a third data rate and the third transceiver is not bonded with any other transceiver.</p> <p>13. The device of claim 9, wherein first and the second transceivers are operable to utilize at least one parameter associated with operation of at least one of the first and second transceivers to reduce a difference in latency between the first and second transceivers.</p> <p><u>’601 Patent (Family 2)</u></p> <p>8. A device comprising:</p> <p>a plurality of transceivers, wherein a first transceiver of the plurality of transceivers is operable to transmit at a first data rate on a first twisted-pair line, and</p> <p>a second transceiver of the plurality of transceivers is simultaneously operable to transmit at a second data rate on a second twisted-pair line, wherein the first data rate and the second data rate are capable of being different and wherein the first and second twisted-pair lines are capable of</p>	

EXHIBIT A – Plaintiff’s Terms and Supporting Evidence

<u>No.</u>	<u>Term</u>	<u>Asserted Claims</u> <u>(Families 2, 3, 6, 9, and 10)</u>	<u>Plaintiff’s Construction and Supporting Evidence</u>
		<p>providing DSL service to a first subscriber, and wherein a third transceiver, of the plurality of transceivers, is simultaneously operable to transmit at a third data rate on a third twisted-pair line, wherein the third twisted-pair line is capable of providing DSL service to a second subscriber, wherein the first and second transceivers are connected to a multi-pair multiplexer.</p> <p>14. The device of claim 8, wherein the first and the second transceivers are operable to utilize at least one parameter associated with operation of at least one of the first and second transceivers to reduce a difference in latency between the first and second transceivers.</p> <p>21. The device of claim 15, wherein the at least two transceivers are operable to utilize at least one parameter associated with operation of at least one of the first and second transceivers to reduce a difference in latency between the first and second transceivers.</p> <p><u>’014 Patent (Family 2)</u></p> <p>1. A device comprising: plurality of transceivers configurable to simultaneously operate with a combination</p>	

EXHIBIT A – Plaintiff’s Terms and Supporting Evidence

<u>No.</u>	<u>Term</u>	<u>Asserted Claims</u> <u>(Families 2, 3, 6, 9, and 10)</u>	<u>Plaintiff’s Construction and Supporting</u> <u>Evidence</u>
		<p>of bonded and unbonded transceivers, wherein a first transceiver of the plurality of transceivers is operable at a first data rate, and a second transceiver of the plurality of transceivers is simultaneously operable at a second data rate that is different than the first data rate, wherein the first and second transceivers are operable as bonded transceivers, and wherein a third transceiver, of the plurality of transceivers, is simultaneously operable at a third data rate, different than the first data rate and the second data rate, and the third transceiver is not bonded with any other transceiver,</p> <p>wherein the first and second transceivers are VDSL transceivers that are operable to transmit Internet Protocol (IP) packets, and wherein the third transceiver is a ADSL transceiver operable to transmit ATM cells.</p> <p><u>’608 Patent (Family 3)</u></p> <p>1. A transceiver comprising: a transmitter portion operable to transmit a first message over a channel, wherein the first message indicates a first maximum number of bytes associated with an inter leaver function of a transmit latency path</p>	

EXHIBIT A – Plaintiff’s Terms and Supporting Evidence

<u>No.</u>	<u>Term</u>	<u>Asserted Claims</u> <u>(Families 2, 3, 6, 9, and 10)</u>	<u>Plaintiff’s Construction and Supporting Evidence</u>
		<p>and a first maximum number of bytes associated with a deinterleaver function of a receive latency path; and</p> <p>a receiver portion operable to determine a change in a channel condition for the channel;</p> <p>the transmitter portion further operable to transmit a second message over the channel after determining the change in the channel condition, wherein the second message indicates a second maximum number of bytes associated with the interleaver function of the transmit latency path and a second maximum number of bytes associated with the deinterleaver function of the receive latency path,</p> <p>wherein the first maximum number of bytes associated with the interleaver function of the transmit latency path is different than the second maximum number of bytes associated with the interleaver function of the transmit latency path, and</p> <p>wherein the first maximum number of bytes associated with the deinterleaver function of the receive latency path is different than the second maximum number of bytes associated with the deinterleaver function of the receive latency path.</p>	

EXHIBIT A – Plaintiff’s Terms and Supporting Evidence

<u>No.</u>	<u>Term</u>	<u>Asserted Claims</u> <u>(Families 2, 3, 6, 9, and 10)</u>	<u>Plaintiff’s Construction and Supporting</u> <u>Evidence</u>
		<p>4. A transceiver comprising:</p> <p>a transmitter portion operable to transmit a first message over a channel at a first time, wherein the first message indicates a first maximum number of bytes associated with an interleaver function of a transmit latency path and a first maximum number of bytes associated with a deinterleaver function of a receive latency path; and</p> <p>a receiver portion operable to determine a change in a channel condition of the channel,</p> <p>wherein the transmitter portion is further operable to transmit a second message over the channel at a second time after determining the change in the channel condition, wherein the second message indicates a second maximum number of bytes associated with the interleaver function of the transmit latency path and a second maximum number of bytes associated with the deinterleaver function of the receive latency path,</p> <p>wherein the first maximum number of bytes associated with the interleaver function of the transmit latency path is different than the second maximum number of bytes associated with the interleaver function of the transmit latency path,</p>	

EXHIBIT A – Plaintiff’s Terms and Supporting Evidence

<u>No.</u>	<u>Term</u>	<u>Asserted Claims</u> <u>(Families 2, 3, 6, 9, and 10)</u>	<u>Plaintiff’s Construction and Supporting</u> <u>Evidence</u>
		<p>wherein the first maximum number of bytes associated with the deinterleaver function of the receive latency path is different than the second maximum number of bytes associated with the deinterleaver function of the receive latency path,</p> <p>wherein the first time is different than the second time, and</p> <p>wherein one or more bytes of memory is used by the interleaver function of the transmitter portion at the first time and the same one or more bytes of the memory are used by the deinterleaver function of the receiver portion at the second time.</p> <p><u>’510 Patent (Family 3)</u></p> <p>21. A device comprising:</p> <p>a transceiver operable to allocate a first portion of shared memory to an interleaver in a transmit latency path and operable allocate a second portion of the shared memory to a deinterleaver in a receiver latency path;</p> <p>the transceiver further operable to transmit to another transceiver information that indicates the shared memory allocation between the interleaver and the deinterleaver, and</p> <p>and operable to update the shared memory allocation between the interleaver and</p>	

EXHIBIT A – Plaintiff’s Terms and Supporting Evidence

<u>No.</u>	<u>Term</u>	<u>Asserted Claims</u> <u>(Families 2, 3, 6, 9, and 10)</u>	<u>Plaintiff’s Construction and Supporting</u> <u>Evidence</u>
		<p>deinterleaver based on changing communication conditions, wherein the changing communications conditions include a change in channel conditions.</p> <p>22. The device of claim 21, wherein the transceiver is further operable to transmit to another transceiver information that indicates the updated shared memory allocation between the interleaver and the deinterleaver.</p> <p><u>’112 Patent (Family 6)</u></p> <p>8. A transceiver comprising: a receiver operable to receiving, during steady-state communication, using a first forward error correction and interleaving parameter (FIP) setting that comprises a forward error correction (FEC) codeword size and a first number of FEC coding parity bytes; and the receiver further operable to switch, during the steady state communication, to receiving using a second FIP setting that comprises a second FEC codeword size that is different than the first FEC code word size and a second number of FEC coding parity bytes that is different than the first number of FEC coding parity bytes,</p>	

EXHIBIT A – Plaintiff’s Terms and Supporting Evidence

<u>No.</u>	<u>Term</u>	<u>Asserted Claims</u> <u>(Families 2, 3, 6, 9, and 10)</u>	<u>Plaintiff’s Construction and Supporting Evidence</u>
		<p>wherein the switching to receiving using the second FEC codeword size and the second number of FEC coding parity bytes is based on a counter reaching a value.</p> <p><u>’577 Patent (Family 9)</u></p> <p>16. An apparatus comprising: a multicarrier transceiver operable to receive at least one packet using deinterleaving, and transmit at least one message without using interleaving, wherein the at least one message includes information that indicates an acknowledgement (ACK) or a negative acknowledgement (NACK) of the at least one packet, wherein the at least one packet comprises one or more PTM-TC codewords.</p> <p>17. The apparatus of claim 16, wherein the transceiver is operable to receive at least one retransmitted packet using interleaving.</p> <p>30. An apparatus comprising: a multicarrier transceiver operable to receive at least one packet using deinterleaving, and transmit at least one message without using interleaving, wherein the at least one message includes information</p>	

EXHIBIT A – Plaintiff’s Terms and Supporting Evidence

<u>No.</u>	<u>Term</u>	<u>Asserted Claims</u> <u>(Families 2, 3, 6, 9, and 10)</u>	<u>Plaintiff’s Construction and Supporting Evidence</u>
		<p>that indicates an acknowledgement (ACK) or a negative acknowledgement (NACK) of the at least one packet, wherein the at least one packet comprises one or more Reed-Solomon codewords.</p> <p>31. The apparatus of claim 30, wherein the transceiver is operable to receive at least one retransmitted packet using interleaving.</p> <p>37. An apparatus comprising: a multicarrier transceiver operable to transmit at least one packet using interleaving, and receive at least one message without using interleaving, wherein the at least one message includes information that indicates an acknowledgement (ACK) or a negative acknowledgement (NACK) of the at least one packet, wherein the at least one packet comprises one or more PTM-TC codewords.</p> <p>38. The apparatus of claim 37, wherein the transceiver is operable to retransmit at least one packet using interleaving.</p> <p>53. An apparatus comprising: a multicarrier transceiver operable to transmit at least one packet using interleaving, and receive at least one message without</p>	

EXHIBIT A – Plaintiff’s Terms and Supporting Evidence

<u>No.</u>	<u>Term</u>	<u>Asserted Claims</u> <u>(Families 2, 3, 6, 9, and 10)</u>	<u>Plaintiff’s Construction and Supporting Evidence</u>
		<p>using interleaving, wherein the at least one message includes information that indicates an acknowledgement (ACK) or a negative acknowledgement (NACK) of the at least one packet, wherein the at least one packet comprises one or more Reed-Solomon codewords.</p> <p>54. The apparatus of claim 53, wherein the transceiver is operable to retransmit at least one packet using interleaving.</p> <p><u>’348 Patent (Family 9)</u></p> <p>1. An apparatus comprising: a multicarrier transceiver including a processor and memory operable to: transmit a packet using a forward error correction encoder and an interleaver, wherein the packet comprises a header field and a plurality of PTM-TC codewords, a plurality of ATM cells or a plurality of Reed-Solomon codewords, and wherein the header field comprises a sequence identifier (SID); and receive a plurality of messages using a forward error correction decoder and without using a deinterleaver, wherein each message of the plurality of messages is received in a different DMT symbol and wherein at least one message of the plural-</p>	

EXHIBIT A – Plaintiff’s Terms and Supporting Evidence

<u>No.</u>	<u>Term</u>	<u>Asserted Claims</u> <u>(Families 2, 3, 6, 9, and 10)</u>	<u>Plaintiff’s Construction and Supporting Evidence</u>
		<p>ity of messages includes an acknowledgement (ACK) or a negative acknowledgement (NACK) of the transmitted packet.</p> <p>3. The apparatus of claim 1, wherein the transceiver is operable to retransmit the packet using the forward error correction encoder and the interleaver.</p> <p>9. An apparatus comprising: a multicarrier transceiver including a processor and memory operable to: receive a packet using a forward error correction decoder and a deinterleaver, wherein the packet comprises a header field and a plurality of PTM-TC codewords, a plurality of ATM cells or a plurality of Reed-Solomon codewords, and wherein the header field comprises a sequence identifier (SID); and transmit a plurality of messages using a forward error correction encoder and without using an interleaver, wherein each message of the plurality of messages is transmitted in a different DMT symbol and wherein at least one message of the plurality of messages includes an acknowledgement (ACK) or a negative acknowledgement (NACK) of the received packet.</p>	

EXHIBIT A – Plaintiff’s Terms and Supporting Evidence

<u>No.</u>	<u>Term</u>	<u>Asserted Claims</u> <u>(Families 2, 3, 6, 9, and 10)</u>	<u>Plaintiff’s Construction and Supporting</u> <u>Evidence</u>
		<p>11. The apparatus of claim 9, wherein the transceiver is operable to receive a retransmitted packet using the forward error correction decoder and the deinterleaver.</p> <p><u>’055 Patent (Family 9)</u></p> <p>11. A transceiver operable to transmit a first type of packet and to transmit a second type of packet, wherein the first type of packet is stored in a retransmission buffer after transmission and the second type of packet is not stored in a retransmission buffer after transmission, and wherein the first and second types of packet comprise a header field that indicates whether a transmitted packet is a first type of packet or a second type of packet, and wherein the header field of the first type of packet comprises a sequence identifier (SID) that is incremented after the first type of packet is transmitted and the header field of the second type of packet does not comprise the SID of the first type of packet.</p> <p><u>’4473 Patent (Family 9)</u></p> <p>1. An apparatus comprising: a multicarrier transceiver including a processor and memory operable to reduce a packet error rate by: transmitting, by the transceiver, a packet using a forward error correction encoder</p>	

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<u>No.</u>	<u>Term</u>	<u>Asserted Claims</u> <u>(Families 2, 3, 6, 9, and 10)</u>	<u>Plaintiff’s Construction and Supporting Evidence</u>
		<p>and an interleaver, wherein the packet comprises a header field and a plurality of bytes, and wherein the header field comprises a sequence identifier (SID); and receiving, by the transceiver, at least one message using a forward error correction decoder and without using a deinterleaver, wherein the at least one message is received in a single discrete multitone (DMT) symbol and wherein the at least one message includes an acknowledgement (ACK) or a negative acknowledgement (NACK) of the transmitted packet,</p> <p>wherein an SNR margin of the at least one message is greater than an SNR margin of the packet; and</p> <p>reducing the packet error rate by retransmitting, by the transceiver and when there is the negative acknowledgement (NACK) in the at least one message, the packet.</p> <p>3. The apparatus of claim 1, wherein the transceiver is operable to retransmit the packet using the forward error correction encoder and the interleaver.</p> <p><u>’354 Patent</u></p> <p>10. A multicarrier communications transceiver operable to:</p>	

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<u>No.</u>	<u>Term</u>	<u>Asserted Claims</u> <u>(Families 2, 3, 6, 9, and 10)</u>	<u>Plaintiff’s Construction and Supporting Evidence</u>
		<p>receive a multicarrier symbol comprising a first plurality of carriers and a second plurality of carriers; receive a first plurality of bits on the first plurality of carriers using a first SNR margin; receive a second plurality of bits on the second plurality of carriers using a second SNR margin; wherein the first plurality of carriers is different than the second plurality of carriers, wherein the first SNR margin is different than the second SNR margin, and wherein the first SNR margin provides more robust than the second SNR margin.</p> <p><u>’988 Patent:</u> 16. An apparatus comprising: a multicarrier communications transceiver operable to demodulate for reception a first plurality of bits from a first carrier using a first Signal to Noise Ratio (SNR) margin and to demodulate for reception a second plurality of bits from a second carrier using a second SNR margin, and to demodulate for reception a third plurality of bits from the first carrier using a third SNR margin, wherein the first SNR margin specifies a first value for an allowable increase in noise without an increase in</p>	

EXHIBIT A – Plaintiff’s Terms and Supporting Evidence

<u>No.</u>	<u>Term</u>	<u>Asserted Claims</u> <u>(Families 2, 3, 6, 9, and 10)</u>	<u>Plaintiff’s Construction and Supporting Evidence</u>
		<p>the bit error rate (BER) associated with the first carrier,</p> <p>wherein the second SNR margin specifies a second value for an allowable increase in noise without an increase in the bit error rate (BER) associated with the second carrier,</p> <p>wherein the third SNR margin specifies a third value for an allowable increase in noise without an increase in the bit error rate (BER) associated with said first carrier,</p> <p>wherein the first SNR margin is different than the second SNR margin,</p> <p>wherein the first SNR margin is different than the third SNR margin, and</p> <p>wherein the first plurality of bits, the second plurality of bits and the third plurality of bits are each different from one another.</p>	

EXHIBIT A – Plaintiff’s Terms and Supporting Evidence**III. FAMILY 1**

<u>No.</u>	<u>Term</u>	<u>Family 1 Asserted Claims</u>	<u>Plaintiff’s Construction and Supporting Evidence</u>
3.	<p>“each bit in the diagnostic message is mapped to at least one DMT symbol”</p> <p>’686 Patent: Claim 17</p> <p>“DMT symbols that are mapped to one bit of the diagnostic message”</p> <p>’686 Patent: Claim 36</p> <p>“at least one bit in the diagnostic message is mapped to at least one DMT symbol”</p> <p>’686 Patent: Claim 40</p>	<p><u>’686 Patent</u></p> <p>17. An information storage media comprising instructions that when executed communicate diagnostic information over a communication channel using multicarrier modulation comprising:</p> <p>instructions that when executed direct a transceiver to receive or transmit an initiate diagnostic mode message; and</p> <p>instructions that when executed transmit a diagnostic message from the transceiver using multicarrier modulation, wherein the diagnostic message comprises a plurality of data variables representing the diagnostic information about the communication channel and each bit in the diagnostic message is mapped to at least one DMT symbol, and wherein one variable comprises an array representing frequency domain received idle channel noise information.</p> <p>36. An information storage media comprising instructions that when executed communicate diagnostic information over a communication channel using multicarrier modulation comprising:</p>	<p>“each bit in the diagnostic message is communicated using a modulation scheme where a DMT symbol (or two or more DMT symbols) represents only a single bit of the diagnostic message”</p> <p>’686 Patent: Claim 17</p> <p>“at least one bit in the diagnostic message is communicated using a modulation scheme where two or more DMT symbols represent only the same single bit of the diagnostic message”</p> <p>’686 Patent: Claim 36</p> <p>“at least one bit in the diagnostic message is communicated using a modulation scheme where a DMT symbol (or two or more DMT symbols) represents only a single bit of the diagnostic message”</p> <p>’686 Patent: Claim 40</p> <p>’686 Patent, cols. 1:34-50, 1:54-2:34, and 3:44-67.</p>

EXHIBIT A – Plaintiff’s Terms and Supporting Evidence

<u>No.</u>	<u>Term</u>	<u>Family 1 Asserted Claims</u>	<u>Plaintiff’s Construction and Supporting Evidence</u>
		<p>instructions that when executed direct a transceiver to receive or transmit an initiate diagnostic mode message; and</p> <p>instructions that when executed transmit from the transceiver a diagnostic message using multicarrier modulation with DMT symbols that are mapped to one bit of the diagnostic message, wherein the diagnostic message comprises a plurality of data variables representing the diagnostic information about the communication channel, and wherein one variable comprises an array representing is frequency domain received idle channel noise information.</p> <p>40. In a multicarrier modulation transceiver, a method of communicating diagnostic information over a communication channel using multicarrier modulation comprising:</p> <p>transmitting, during a diagnostic mode, a diagnostic message using multicarrier modulation, wherein the diagnostic message comprises a plurality of data variables representing the diagnostic information about the communication channel and at least one bit in the diagnostic message is mapped to at least one DMT symbol, wherein one variable comprises an array</p>	<p>ITU-T G.993.2 (02/2019) at § 12.4.1.1</p> <p>Declaration of Dr. Vijay Madiseti.</p>

EXHIBIT A – Plaintiff’s Terms and Supporting Evidence

<u>No.</u>	<u>Term</u>	<u>Family 1 Asserted Claims</u>	<u>Plaintiff’s Construction and Supporting Evidence</u>
		representing frequency domain received idle channel noise information.	
4.	<p>“array representing frequency domain received idle channel noise information”</p> <p>’686 Patent: Claims 17, 36, 40.</p>	<p><u>’686 Patent</u></p> <p>17. An information storage media comprising instructions that when executed communicate diagnostic information over a communication channel using multicarrier modulation comprising:</p> <p>instructions that when executed direct a transceiver to receive or transmit an initiate diagnostic mode message; and</p> <p>instructions that when executed transmit a diagnostic message from the transceiver using multicarrier modulation, wherein the diagnostic message comprises a plurality of data variables representing the diagnostic information about the communication channel and each bit in the diagnostic message is mapped to at least one DMT symbol, and wherein one variable comprises an array representing frequency domain received idle channel noise information.</p> <p>36. An information storage media comprising instructions that when executed communicate diagnostic information over a communication channel using multicarrier modulation comprising:</p>	<p>“ordered set of values representative of noise in the frequency domain that was received by a transceiver on respective sub-channels in the absence of a transmission signal on the received channel”</p> <p>’686 Patent, cols. 1:34–50, 4:1-50, and 5:54-6:9.</p> <p>Declaration of Dr. Vijay Madiseti.</p>

EXHIBIT A – Plaintiff’s Terms and Supporting Evidence

<u>No.</u>	<u>Term</u>	<u>Family 1 Asserted Claims</u>	<u>Plaintiff’s Construction and Supporting Evidence</u>
		<p>instructions that when executed direct a transceiver to receive or transmit an initiate diagnostic mode message; and</p> <p>instructions that when executed transmit from the transceiver a diagnostic message using multicarrier modulation with DMT symbols that are mapped to one bit of the diagnostic message, wherein the diagnostic message comprises a plurality of data variables representing the diagnostic information about the communication channel, and wherein one variable comprises an array representing is frequency domain received idle channel noise information.</p> <p>40. In a multicarrier modulation transceiver, a method of communicating diagnostic information over a communication channel using multicarrier modulation comprising:</p> <p>transmitting, during a diagnostic mode, a diagnostic message using multicarrier modulation, wherein the diagnostic message comprises a plurality of data variables representing the diagnostic information about the communication channel and at least one bit in the diagnostic message is mapped to at least one DMT symbol, wherein one variable comprises an array representing</p>	

EXHIBIT A – Plaintiff’s Terms and Supporting Evidence

<u>No.</u>	<u>Term</u>	<u>Family 1 Asserted Claims</u>	<u>Plaintiff’s Construction and Supporting Evidence</u>
		frequency domain received idle channel noise information.	

EXHIBIT A – Plaintiff’s Terms and Supporting Evidence**IV. FAMILY 2**

<u>No.</u>	<u>Term</u>	<u>Family 2 Asserted Claims</u>	<u>Plaintiff’s Construction and Supporting Evidence</u>
5.	<p>“plurality of bonded transceivers”</p> <p><u>Family 2:</u> ’881 Patent: Claims 17, 25, 33, 37*</p> <p>* Defendants also identified claims 18, 21, 23, 26, 29, and 31 as possessing this term. These dependent claims do not contain the term “plurality of bonded transceivers” except by virtue of the independent claim.</p>	<p><u>’881 Patent</u></p> <p>17. A plurality of bonded transceivers, each bonded transceiver utilizing at least one transmission parameter value to reduce a difference in latency between the bonded transceivers, wherein a data rate for a first of the bonded transceivers is different than a data rate for a second of the bonded transceivers.</p> <p>25. A plurality of bonded transceivers, each bonded transceiver selecting at least one transmission parameter value to reduce a difference in latency between the bonded transceivers, wherein a data rate for a first of the bonded transceivers is different than a data rate for a second of the bonded transceivers.</p> <p>33. A storage media having computer executable instructions stored thereon that: utilize at least one transmission parameter value, for each transceiver in a plurality of bonded transceivers, to reduce a difference in latency between the bonded transceivers, wherein a data rate for a first of the plurality of bonded transceivers is different than a data rate for a second of the plurality of bonded transceivers.</p>	<p>“two or more transceivers located on the same side of two or more physical links where each transceiver is configurable to transmit or receive a different portion of the same bit stream via a different one of the physical links”</p> <p>’881 patent, Figs. 2-12, cols. 1:42-2:19, 3:58-5:9, 5:22-67, 10:54-58, 11:31-34.</p> <p>Declaration of Dr. Todor Cooklev.</p>

EXHIBIT A – Plaintiff’s Terms and Supporting Evidence

<u>No.</u>	<u>Term</u>	<u>Family 2 Asserted Claims</u>	<u>Plaintiff’s Construction and Supporting Evidence</u>
		<p>37. A storage media having computer executable instructions stored thereon that: select at least one transmission parameter value, for each transceiver in a plurality of bonded transceivers, to reduce a difference in latency between the bonded transceivers, wherein a data rate of a first of the plurality of bonded transceivers is different than a data rate of a second of the plurality of bonded transceivers.</p>	
6.	<p>“reduce a difference in latency between the bonded transceivers”</p> <p><u>Family 2:</u> ’881 Patent: Claims 17, 25, 33, 37*</p> <p>* Defendants also identified claims 26, 29, and 31 as possessing this term. These dependent claims do not contain the term “reduce a difference in latency between the bonded transceivers” except by virtue of the independent claim.</p>	<p><u>’881 Patent</u></p> <p>17. A plurality of bonded transceivers, each bonded transceiver utilizing at least one transmission parameter value to reduce a difference in latency between the bonded transceivers, wherein a data rate for a first of the bonded transceivers is different than a data rate for a second of the bonded transceivers.</p> <p>25. A plurality of bonded transceivers, each bonded transceiver selecting at least one transmission parameter value to reduce a difference in latency between the bonded transceivers, wherein a data rate for a first of the bonded transceivers is different than a data rate for a second of the bonded transceivers.</p> <p>33. A storage media having computer executable instructions stored thereon that:</p>	<p>“reduce a difference in configuration latency”</p> <p>’881 Patent, Fig. 15, cols. 5:23-42, 6:1-35, 6:56-7:36, and 10:40-47.</p> <p>Declaration of Dr. Todor Cooklev.</p>

EXHIBIT A – Plaintiff’s Terms and Supporting Evidence

<u>No.</u>	<u>Term</u>	<u>Family 2 Asserted Claims</u>	<u>Plaintiff’s Construction and Supporting Evidence</u>
		<p>utilize at least one transmission parameter value, for each transceiver in a plurality of bonded transceivers, to reduce a difference in latency between the bonded transceivers, wherein a data rate for a first of the plurality of bonded transceivers is different than a data rate for a second of the plurality of bonded transceivers.</p> <p>37. A storage media having computer executable instructions stored thereon that: select at least one transmission parameter value, for each transceiver in a plurality of bonded transceivers, to reduce a difference in latency between the bonded transceivers, wherein a data rate of a first of the plurality of bonded transceivers is different than a data rate of a second of the plurality of bonded transceivers.</p>	
7.	“each bonded transceiver [utilizing/selecting] at least one transmission parameter value to reduce a difference in latency between the bonded transceivers” (Claims 17 and 25) / “[utilize/select] at least one transmission parameter value, for each transceiver	<p><u>’881 Patent</u></p> <p>17. A plurality of bonded transceivers, each bonded transceiver utilizing at least one transmission parameter value to reduce a difference in latency between the bonded transceivers, wherein a data rate for a first of the bonded transceivers is different than a data rate for a second of the bonded transceivers.</p>	<p>Plain and ordinary meaning. No construction necessary.</p> <p>The term “reduce a difference in latency between the bonded transceivers” means “reduce a difference in configuration latency”</p> <p>’881 Patent, Fig. 15, cols. 5:23-42, 6:1-35, 6:56-7:36, and 10:40-47.</p>

EXHIBIT A – Plaintiff’s Terms and Supporting Evidence

<u>No.</u>	<u>Term</u>	<u>Family 2 Asserted Claims</u>	<u>Plaintiff’s Construction and Supporting Evidence</u>
	<p>in a plurality of bonded transceivers, to reduce a difference in latency between the bonded transceivers” (Claim 33 and 37)</p> <p><u>Family 2:</u> ’881 Patent: Claims 17 (“utilizing”), 25 (“selecting”), 33 (“utilize”), 37 (“select”)*</p> <p>* Defendants also identified claims 26, 29, and 31 as possessing this term. These dependent claims do not contain the term except by virtue of the independent claim.</p>	<p>25. A plurality of bonded transceivers, each bonded transceiver selecting at least one transmission parameter value to reduce a difference in latency between the bonded transceivers, wherein a data rate for a first of the bonded transceivers is different than a data rate for a second of the bonded transceivers.</p> <p>33. A storage media having computer executable instructions stored thereon that: utilize at least one transmission parameter value, for each transceiver in a plurality of bonded transceivers, to reduce a difference in latency between the bonded transceivers, wherein a data rate for a first of the plurality of bonded transceivers is different than a data rate for a second of the plurality of bonded transceivers.</p> <p>37. A storage media having computer executable instructions stored thereon that: select at least one transmission parameter value, for each transceiver in a plurality of bonded transceivers, to reduce a difference in latency between the bonded transceivers, wherein a data rate of a first of the plurality of bonded transceivers is different than a data rate of a</p>	<p>Declaration of Dr. Todor Cooklev.</p>

EXHIBIT A – Plaintiff’s Terms and Supporting Evidence

<u>No.</u>	<u>Term</u>	<u>Family 2 Asserted Claims</u>	<u>Plaintiff’s Construction and Supporting Evidence</u>
		second of the plurality of bonded transceivers.	

EXHIBIT A – Plaintiff’s Terms and Supporting Evidence**V. FAMILY 3**

<u>No.</u>	<u>Term</u>	<u>Family 3 Asserted Claims</u>	<u>Plaintiff’s Construction and Supporting Evidence</u>
8.	<p>“shared memory” / “sharing the memory” / “operable to be shared” / “sharing”</p> <p><u>Family 3:</u> ’882 Patent: Claims 9 and 13 (“shared memory”) ’048 Patent: Claims 1 and 5 (“shared memory”) ’5,473 Patent: Claim 10 (“sharing the memory”) ’608 Patent: Claim 2 (“operable to be shared / sharing”) ’510 Patent: Claim 21 (“shared memory”)</p>	<p><u>’882 Patent</u> 9. A system that allocates shared memory comprising: a transceiver that performs: transmitting or receiving a message during initialization specifying a maximum number of bytes of memory that are available to be allocated to an interleaver, determining an amount of memory required by the inter leaver to interleave a first plurality of Reed Solomon (RS) coded data bytes within a shared memory; allocating a first number of bytes of the shared memory to the interleaver to interleave the first plurality of ReedSolomon (RS) coded data bytes for transmission at a first data rate, wherein the allocated memory for the interleaver does not exceed the maximum number of bytes specified in the message; allocating a second number of bytes of the shared memory to a deinterleaver to deinterleave a second plurality of RS coded data bytes received at a second data rate; and interleaving the first plurality of RS coded data bytes within the shared memory allocated to the interleaver and deinter-</p>	<p>“common memory used by at least two functions, where a portion of the memory can be used by either one of the functions”</p> <p>’882 Patent, Abstract, Figs. 1-3 (Shared Memory 120), 1:55-2:9, 2:27-44, 4:1-13, 4:23-65, 5:10-17, 5:33-57, 5:65-6:64, 7:7-25and 9:28-37</p> <p>Declaration of Dr. Todor Cooklev.</p>

EXHIBIT A – Plaintiff’s Terms and Supporting Evidence

<u>No.</u>	<u>Term</u>	<u>Family 3 Asserted Claims</u>	<u>Plaintiff’s Construction and Supporting Evidence</u>
		<p>leaving the second plurality of RS coded data bytes within the shared memory allocated to the deinterleaver, wherein the shared memory allocated to the interleaver is used at the same time as the shared memory allocated to the deinterleaver.</p> <p>13. A system that allocates shared memory comprising:</p> <p>a transceiver that performs:</p> <p>transmitting or receiving a message during initialization specifying a maximum number of bytes of memory that are available to be allocated to a deinterleaver;</p> <p>determining an amount of memory required by the deinterleaver to deinterleave a first plurality of Reed Solomon (RS) coded data bytes within a shared memory;</p> <p>allocating a first number of bytes of the shared memory to the deinterleaver to deinterleave a first plurality of Reed Solomon (RS) coded databytes for transmission at a first data rate, wherein the allocated memory for the deinterleaver does not exceed the maximum number of bytes specified in the message;</p> <p>allocating a second number of bytes of the shared memory to an interleaver to in-</p>	

EXHIBIT A – Plaintiff’s Terms and Supporting Evidence

<u>No.</u>	<u>Term</u>	<u>Family 3 Asserted Claims</u>	<u>Plaintiff’s Construction and Supporting Evidence</u>
		<p>terleave a second plurality of RS coded data bytes received at a second data rate; and deinterleaving the first plurality of RS coded data bytes within the shared memory allocated to the deinterleaver and interleaving the second plurality of RS coded data bytes within the sh[a]red memory allocated to the interleaver, wherein the shared memory allocated to the deinterleaver is used at the same time as the shared memory allocated to the interleaver.</p> <p><u>’048 Patent</u></p> <p>1. A system that allocates shared memory comprising: a transceiver that is capable of transmitting or receiving a message during initialization specifying a maximum number of bytes of memory that are available to be allocated to an interleaver; determining an amount of memory required by the interleaver to interleave a first plurality of Reed Solomon (RS) coded data bytes within the shared memory; allocating a first number of bytes of the shared memory to the interleaver to interleave the first plurality of Reed Solo-</p>	

EXHIBIT A – Plaintiff’s Terms and Supporting Evidence

<u>No.</u>	<u>Term</u>	<u>Family 3 Asserted Claims</u>	<u>Plaintiff’s Construction and Supporting Evidence</u>
		<p>mon (RS) coded data bytes for transmission at a first data rate, wherein the allocated memory for the interleaver does not exceed the maximum number of bytes specified in the message; allocating a second number of bytes of the shared memory to a deinterleaver to deinterleave a second plurality of RS coded data bytes received at a second data rate; and interleaving the first plurality of RS coded data bytes within the shared memory allocated to the interleaver and deinterleaving the second plurality of RS coded data bytes within the shared memory allocated to the deinterleaver, wherein the shared memory allocated to the interleaver is used at the same time as the shared memory allocated to the deinterleaver.</p> <p>5. A system that allocates shared memory comprising: a transceiver that is capable of: transmitting or receiving a message during initialization specifying a maximum number of bytes of memory that are available to be allocated to a deinterleaver;</p>	

EXHIBIT A – Plaintiff’s Terms and Supporting Evidence

<u>No.</u>	<u>Term</u>	<u>Family 3 Asserted Claims</u>	<u>Plaintiff’s Construction and Supporting Evidence</u>
		<p>determining an amount of memory required by the deinterleaver to deinterleave a first plurality of Reed Solomon (RS) coded data bytes within the shared memory;</p> <p>allocating a first number of bytes of the shared memory to the deinterleaver to deinterleave a first plurality of ReedSolomon (RS) coded data bytes for transmission at a first data rate, wherein the allocated memory for the deinterleaver does not exceed the maximum number of bytes specified in the message;</p> <p>allocating a second number of bytes of the shared memory to an interleaver to interleave a second plurality of RS coded data bytes received at a second data rate; and</p> <p>deinterleaving the first plurality of RS coded data bytes within the shared memory allocated to the deinterleaver and interleaving the second plurality of RS coded data bytes within the shared memory allocated to the interleaver, wherein the shared memory allocated to the deinterleaver is used at the same time as the shared memory allocated to the interleaver.</p> <p><u>'5473 Patent</u></p>	

EXHIBIT A – Plaintiff’s Terms and Supporting Evidence

<u>No.</u>	<u>Term</u>	<u>Family 3 Asserted Claims</u>	<u>Plaintiff’s Construction and Supporting Evidence</u>
		<p>10. A multicarrier communications transceiver with a shared memory, the transceiver capable of:</p> <p style="padding-left: 40px;">sharing the memory between an interleaver in a first latency path and a deinterleaver in a second latency path; and transmitting or receiving, during initialization of the transceiver, a message indicating how the shared memory is to be used by the interleaver or the deinterleaver.</p> <p style="text-align: center;"><u>’608 Patent</u></p> <p>2. The transceiver of claim 1, further comprising a memory wherein the memory is operable to be shared between the interleaver function of the transmitter portion associated with the transmit latency path and the deinterleaver function of the receiver portion associated with the receive latency path, wherein the first maximum number of bytes associated with the interleaver function is used to determine how much memory is used by the interleaver function and wherein the first maximum number of bytes associated with the deinterleaver function is used to determine how much memory is used by the deinterleaver function,</p> <p style="padding-left: 40px;">wherein the sharing comprises using a first portion of the memory for the interleaver function and simultaneously using a sec-</p>	

EXHIBIT A – Plaintiff’s Terms and Supporting Evidence

<u>No.</u>	<u>Term</u>	<u>Family 3 Asserted Claims</u>	<u>Plaintiff’s Construction and Supporting Evidence</u>
		<p>ond portion of the memory, different than the first portion, for the deinterleaver function, and the first and second portions of the memory are configurable such that one or more bytes of the memory can be used by the interleaver function at one particular time and the same one or more bytes of the memory can be used by the deinterleaver function at a second time, different than the first time.</p> <p style="text-align: center;"><u>’510 Patent</u></p> <p>21. A device comprising: a transceiver operable to allocate a first portion of shared memory to an interleaver in a transmit latency path and operable allocate a second portion of the shared memory to a deinterleaver in a receiver latency path; the transceiver further operable to transmit to another transceiver information that indicates the shared memory allocation between the interleaver and the deinterleaver; and and operable to update the shared memory allocation between the interleaver and deinterleaver based on changing communication conditions, wherein the changing communications conditions include a change in channel conditions.</p>	

EXHIBIT A – Plaintiff’s Terms and Supporting Evidence

<u>No.</u>	<u>Term</u>	<u>Family 3 Asserted Claims</u>	<u>Plaintiff’s Construction and Supporting Evidence</u>
9.	<p>“wherein the generated message indicates how the memory has been allocated between the [first deinterleaving / interleaving] function and the [second] deinterleaving function”</p> <p><u>Family 3:</u></p> <p>’5473 Patent: Claim 28</p>	<p><u>’5473 Patent</u></p> <p>28. An apparatus comprising: a multicarrier communications transceiver that is configured to generate a message during an initialization of the transceiver, perform an interleaving function associated with a first latency path, and perform a deinterleaving function associated with a second latency path, the transceiver being associated with a memory, wherein at least a portion of the memory may be allocated to the interleaving function or the deinterleaving function at any one particular time and wherein the generated message indicates how the memory has been allocated between the interleaving function and the deinterleaving function.</p>	<p>Plain and ordinary meaning. No construction necessary.</p> <p>’4473 patent), Fig. 3 (S320), Fig. 4 (S420 and S470), 4:8-16, 4:27-40, 5:8-20, 5:38-60, 5:63-6:8, 7:1-6, 8:12-54, 9:1-21, and 9:31-40.</p> <p>Declaration of Dr. Todor Cooklev.</p>
10.	<p>“a message indicating how the shared memory is to be used by the interleaver or the deinterleaver”</p> <p><u>Family 3:</u></p> <p>’5473 Patent: Claim 10</p>	<p><u>’5473 Patent</u></p> <p>10. A multicarrier communications transceiver with a shared memory, the transceiver capable of: sharing the memory between an interleaver in a first latency path and a deinterleaver in a second latency path; and transmitting or receiving, during initialization of the transceiver, a message indicat-</p>	<p>Plain and ordinary meaning. No construction necessary.</p> <p>’4473 patent), Fig. 3 (S320), Fig. 4 (S420 and S470), 4:8-16, 4:27-40, 5:8-20, 5:38-60, 5:63-6:8, 7:1-6, 8:12-54, 9:1-21, and 9:31-40.</p> <p>Declaration of Dr. Todor Cooklev</p>

EXHIBIT A – Plaintiff’s Terms and Supporting Evidence

<u>No.</u>	<u>Term</u>	<u>Family 3 Asserted Claims</u>	<u>Plaintiff’s Construction and Supporting Evidence</u>
		ing how the shared memory is to be used by the interleaver or the deinterleaver.	
11.	<p>“specifying a maximum number of bytes of memory that are available to be allocated to [a/an interleaver/deinterleaver]”</p> <p><u>Family 3:</u> ’882 Patent: Claims 9, 13 ’048 Patent: Claims 1, 5</p>	<p><u>’882 Patent</u></p> <p>9. A system that allocates shared memory comprising: a transceiver that performs: transmitting or receiving a message during initialization specifying a maximum number of bytes of memory that are available to be allocated to an interleaver, determining an amount of memory required by the interleaver to interleave a first plurality of Reed Solomon (RS) coded data bytes within a shared memory; allocating a first number of bytes of the shared memory to the interleaver to interleave the first plurality of ReedSolomon (RS) coded data bytes for transmission at a first data rate, wherein the allocated memory for the interleaver does not exceed the maximum number of bytes specified in the message; allocating a second number of bytes of the shared memory to a deinterleaver to deinterleave a second plurality of RS</p>	Plain and ordinary meaning. No construction necessary.

EXHIBIT A – Plaintiff’s Terms and Supporting Evidence

<u>No.</u>	<u>Term</u>	<u>Family 3 Asserted Claims</u>	<u>Plaintiff’s Construction and Supporting Evidence</u>
		<p>coded data bytes received at a second data rate; and interleaving the first plurality of RS coded data bytes within the shared memory allocated to the interleaver and deinterleaving the second plurality of RS coded data bytes within the shared memory allocated to the deinterleaver, wherein the shared memory allocated to the interleaver is used at the same time as the shared memory allocated to the deinterleaver.</p> <p>13. A system that allocates shared memory comprising: a transceiver that performs: transmitting or receiving a message during initialization specifying a maximum number of bytes of memory that are available to be allocated to a deinterleaver; determining an amount of memory required by the deinterleaver to deinterleave a first plurality of Reed Solomon (RS) coded data bytes within a shared memory; allocating a first number of bytes of the shared memory to the deinterleaver to deinterleave a first plurality of Reed Solomon (RS) coded databytes for trans-</p>	

EXHIBIT A – Plaintiff’s Terms and Supporting Evidence

<u>No.</u>	<u>Term</u>	<u>Family 3 Asserted Claims</u>	<u>Plaintiff’s Construction and Supporting Evidence</u>
		<p>mission at a first data rate, wherein the allocated memory for the deinterleaver does not exceed the maximum number of bytes specified in the message; allocating a second number of bytes of the shared memory to an interleaver to interleave a second plurality of RS coded data bytes received at a second data rate; and deinterleaving the first plurality of RS coded data bytes within the shared memory allocated to the deinterleaver and interleaving the second plurality of RS coded data bytes within the sh[a]red memory allocated to the interleaver, wherein the shared memory allocated to the deinterleaver is used at the same time as the shared memory allocated to the interleaver.</p> <p style="text-align: center;"><u>'048 Patent</u></p> <p>1. A system that allocates shared memory comprising: a transceiver that is capable of transmitting or receiving a message during initialization specifying a maximum number of bytes of memory that are available to be allocated to an interleaver;</p>	

EXHIBIT A – Plaintiff’s Terms and Supporting Evidence

<u>No.</u>	<u>Term</u>	<u>Family 3 Asserted Claims</u>	<u>Plaintiff’s Construction and Supporting Evidence</u>
		<p>determining an amount of memory required by the interleaver to interleave a first plurality of Reed Solomon (RS) coded data bytes within the shared memory;</p> <p>allocating a first number of bytes of the shared memory to the interleaver to interleave the first plurality of Reed Solomon (RS) coded data bytes for transmission at a first data rate, wherein the allocated memory for the interleaver does not exceed the maximum number of bytes specified in the message;</p> <p>allocating a second number of bytes of the shared memory to a deinterleaver to deinterleave a second plurality of RS coded data bytes received at a second data rate; and</p> <p>interleaving the first plurality of RS coded data bytes within the shared memory allocated to the interleaver and deinterleaving the second plurality of RS coded data bytes within the shared memory allocated to the deinterleaver, wherein the shared memory allocated to the interleaver is used at the same time as the shared memory allocated to the deinterleaver.</p>	

EXHIBIT A – Plaintiff’s Terms and Supporting Evidence

<u>No.</u>	<u>Term</u>	<u>Family 3 Asserted Claims</u>	<u>Plaintiff’s Construction and Supporting Evidence</u>
		<p>5. A system that allocates shared memory comprising:</p> <ul style="list-style-type: none"> a transceiver that is capable of: <ul style="list-style-type: none"> transmitting or receiving a message during initialization specifying a maximum number of bytes of memory that are available to be allocated to a deinter-leaver; determining an amount of memory required by the deinterleaver to deinterleave a first plurality of Reed Solomon (RS) coded data bytes within the shared memory; allocating a first number of bytes of the shared memory to the deinterleaver to deinterleave a first plurality of ReedSolomon (RS) coded data bytes for transmission at a first data rate, wherein the allocated memory for the deinterleaver does not exceed the maximum number of bytes specified in the message; allocating a second number of bytes of the shared memory to an interleaver to interleave a second plurality of RS coded data bytes received at a second data rate; and deinterleaving the first plurality of RS coded data bytes within the shared memory allocated to the deinterleaver and interleaving the second plurality of 	

EXHIBIT A – Plaintiff’s Terms and Supporting Evidence

<u>No.</u>	<u>Term</u>	<u>Family 3 Asserted Claims</u>	<u>Plaintiff’s Construction and Supporting Evidence</u>
		RS coded data bytes within the shared memory allocated to the interleaver, wherein the shared memory allocated to the deinterleaver is used at the same time as the shared memory allocated to the interleaver.	

EXHIBIT A – Plaintiff’s Terms and Supporting Evidence**VI. FAMILY 4**

<u>No.</u>	<u>Term</u>	<u>Family 4 Asserted Claims</u>	<u>Plaintiff’s Construction and Supporting Evidence</u>
12.	<p>“phase characteristic(s)”</p> <p>or</p> <p>“each carrier signal has a phase characteristic associated with the bit stream”</p> <p><u>Family 4:</u> ’008 Patent: Claim 14</p>	<p><u>’008 Patent</u></p> <p>14. A multicarrier system including a first transceiver that uses a plurality of carrier signals for modulating a bit stream, wherein each carrier signal has a phase characteristic associated with the bit stream, the transceiver capable of:</p> <p>associating each carrier signal with a value determined independently of any bit value of the bit stream carried by that respective carrier signal, the value associated with each carrier signal determined using a pseudo random number generator, computing a phase shift for each carrier signal based on the value associated with that carrier signal; and</p> <p>combining the phase shift computed for each respective carrier signal with the phase characteristic of that carrier signal to substantially scramble the phase characteristics of the plurality of carrier signals, wherein multiple carrier signals corresponding to the scrambled carrier signals are used by the first transceiver to modulate the same bit value.</p>	<p>“one or more values that represent the angular aspect of a carrier signal”</p> <p>’008 Patent), Title, Abstract, 2:28–30, 2:34–3:3, 4:10-12, 4:29–63, 5:25–31, FIGS. 1 and 2.</p> <p>Figure 22 of the T1.413-1998 standard</p> <p>Declaration of Dr. Vijay Madiseti.</p>

EXHIBIT A – Plaintiff’s Terms and Supporting Evidence

<u>No.</u>	<u>Term</u>	<u>Family 4 Asserted Claims</u>	<u>Plaintiff’s Construction and Supporting Evidence</u>
13.	<p>“substantially scramble the phase characteristics of the plurality of carrier signal”</p> <p><u>Family 4:</u></p> <p>’008 Patent: Claim 14</p>	<p><u>’008 Patent</u></p> <p>14. A multicarrier system including a first transceiver that uses a plurality of carrier signals for modulating a bit stream, wherein each carrier signal has a phase characteristic associated with the bit stream, the transceiver capable of:</p> <p>associating each carrier signal with a value determined independently of any bit value of the bit stream carried by that respective carrier signal, the value associated with each carrier signal determined using a pseudo random number generator, computing a phase shift for each carrier signal based on the value associated with that carrier signal; and</p> <p>combining the phase shift computed for each respective carrier signal with the phase characteristic of that carrier signal to substantially scramble the phase characteristics of the plurality of carrier signals, wherein multiple carrier signals corresponding to the scrambled carrier signals are used by the first transceiver to modulate the same bit value.</p>	<p>“adjust the phase characteristics of the carrier signals by varying amounts to produce a transmission signal with a reduced peak to-average power ratio (PAR)”</p> <p>’008 Patent, Abstract, 2:15-30, 2:44–47, 2:66–3:3, 4:3238, FIGS. 1 and 2.</p> <p>Declaration of Dr. Vijay Madiseti.</p>
14.	<p>“same bit value”</p> <p><u>Family 4:</u></p> <p>’008 Patent: Claim 14</p>	<p><u>’008 Patent</u></p> <p>14. A multicarrier system including a first transceiver that uses a plurality of carrier signals for modulating a bit stream, wherein</p>	<p>“value of the same bit”</p> <p>’008 Patent, Cols. 9:15-28.</p>

EXHIBIT A – Plaintiff’s Terms and Supporting Evidence

<u>No.</u>	<u>Term</u>	<u>Family 4 Asserted Claims</u>	<u>Plaintiff’s Construction and Supporting Evidence</u>
		<p>each carrier signal has a phase characteristic associated with the bit stream, the transceiver capable of:</p> <p>associating each carrier signal with a value determined independently of any bit value of the bit stream carried by that respective carrier signal, the value associated with each carrier signal determined using a pseudo random number generator, computing a phase shift for each carrier signal based on the value associated with that carrier signal; and</p> <p>combining the phase shift computed for each respective carrier signal with the phase characteristic of that carrier signal to substantially scramble the phase characteristics of the plurality of carrier signals, wherein multiple carrier signals corresponding to the scrambled carrier signals are used by the first transceiver to modulate the same bit value.</p>	Declaration of Dr. Vijay Madiseti.
15.	<p>“multiple carrier signals corresponding to the scrambled carrier signals are used by the first multicarrier transceiver to modulate the same bit value”</p> <p><u>Family 4:</u></p>	<p><u>’008 Patent</u></p> <p>14. A multicarrier system including a first transceiver that uses a plurality of carrier signals for modulating a bit stream, wherein each carrier signal has a phase characteristic associated with the bit stream, the transceiver capable of:</p>	<p>“a first carrier signal is used by the first multicarrier transceiver to modulate the value of a bit of the received bit stream and at least one more carrier signal is used by the first multi carrier transceiver to modulate the value of the same bit of the received bit stream, wherein the carrier signals correspond to the plurality of</p>

EXHIBIT A – Plaintiff’s Terms and Supporting Evidence

<u>No.</u>	<u>Term</u>	<u>Family 4 Asserted Claims</u>	<u>Plaintiff’s Construction and Supporting Evidence</u>
	’008 Patent: Claim 14	<p>associating each carrier signal with a value determined independently of any bit value of the bit stream carried by that respective carrier signal, the value associated with each carrier signal determined using a pseudo random number generator, computing a phase shift for each carrier signal based on the value associated with that carrier signal; and</p> <p>combining the phase shift computed for each respective carrier signal with the phase characteristic of that carrier signal to substantially scramble the phase characteristics of the plurality of carrier signals, wherein multiple carrier signals corresponding to the scrambled carrier signals are used by the first transceiver to modulate the same bit value.</p>	<p>phase-shifted and scrambled carrier signals”</p> <p>’008 Patent, 2:16–25, 3:57–62, 4:43–47, FIG. 1.</p> <p>Declaration of Dr. Vijay Madiseti.</p>
16.	<p>“computing a phase shift for each carrier signal”</p> <p><u>Family 4:</u> ’008 Patent: Claim 14</p>	<p><u>’008 Patent</u></p> <p>14. A multicarrier system including a first transceiver that uses a plurality of carrier signals for modulating a bit stream, wherein each carrier signal has a phase characteristic associated with the bit stream, the transceiver capable of:</p> <p>associating each carrier signal with a value determined independently of any bit value of the bit stream carried by that re-</p>	<p>Plain and ordinary meaning. No construction necessary.</p> <p>’627 at 2:33-40, 2:55-65, 4:33-36, 4:52-54, 5:1-8, 5:8-21, 6:32-35, 6:4749, 6:59-62, Figure 2.</p> <p>Declaration of Dr. Vijay Madiseti.</p>

EXHIBIT A – Plaintiff’s Terms and Supporting Evidence

<u>No.</u>	<u>Term</u>	<u>Family 4 Asserted Claims</u>	<u>Plaintiff’s Construction and Supporting Evidence</u>
		<p>spective carrier signal, the value associated with each carrier signal determined using a pseudo random number generator, computing a phase shift for each carrier signal based on the value associated with that carrier signal; and</p> <p>combining the phase shift computed for each respective carrier signal with the phase characteristic of that carrier signal to substantially scramble the phase characteristics of the plurality of carrier signals, wherein multiple carrier signals corresponding to the scrambled carrier signals are used by the first transceiver to modulate the same bit value.</p>	
17.	<p>“combining the phase shift computed for each respective carrier signal with the phase characteristic of that carrier signal”</p> <p><u>Family 4:</u> ’008 Patent: Claim 14</p>	<p><u>’008 Patent</u></p> <p>14. A multicarrier system including a first transceiver that uses a plurality of carrier signals for modulating a bit stream, wherein each carrier signal has a phase characteristic associated with the bit stream, the transceiver capable of:</p> <p>associating each carrier signal with a value determined independently of any bit value of the bit stream carried by that respective carrier signal, the value associated with each carrier signal determined using a pseudo random number generator, computing a phase shift for each carrier</p>	<p>Plain and ordinary meaning. No construction necessary.</p> <p>’008 patent, 1:40-45, 4:43-47, 3:57-62, 6:46-8:17.</p> <p>Declaration of Dr. Vijay Madiseti.</p>

EXHIBIT A – Plaintiff’s Terms and Supporting Evidence

<u>No.</u>	<u>Term</u>	<u>Family 4 Asserted Claims</u>	<u>Plaintiff’s Construction and Supporting Evidence</u>
		<p>signal based on the value associated with that carrier signal; and</p> <p>combining the phase shift computed for each respective carrier signal with the phase characteristic of that carrier signal to substantially scramble the phase characteristics of the plurality of carrier signals, wherein multiple carrier signals corresponding to the scrambled carrier signals are used by the first transceiver to modulate the same bit value.</p>	

EXHIBIT A – Plaintiff’s Terms and Supporting Evidence**VII. FAMILY 6**

<u>No.</u>	<u>Term</u>	<u>Family 6 Asserted Claims</u>	<u>Plaintiff’s Construction and Supporting Evidence</u>
18.	<p>“steady-state communication”</p> <p><u>Family 6:</u> ’835 Patent: Claim 8 and 24 ’112 Patent: Claim 8</p>	<p><u>’835 Patent</u></p> <p>8. An apparatus configurable to adapt forward error correction and interleaver parameter (FIP) settings during steady-state communication or initialization comprising: a transceiver, including a processor, configurable to: transmit a signal using a first FIP setting, transmit a flag signal, and switch to using for transmission, a second FIP setting following transmission of the flag signal, wherein: the first FIP setting comprises at least one first FIP value, the second FIP setting comprises at least one second FIP value, different than the first FIP value, and the switching occurs on a pre-defined forward error correction codeword boundary following the flag signal.</p> <p>24. An apparatus configurable to adapt forward error correction and interleaver parameter (FIP) settings during steady-state communication or initialization comprising: a transceiver, including a processor, configurable to: receive a signal using a first FIP setting, receive a flag signal, and Switch to using</p>	<p>“Showtime”</p> <p>’835 Patent, Abstract, Figs. 1-7, Cols. 2:43-49, 3:48-58, 4:3-54, 5:7-15, 6:45-51, 8:21-49, 9:15-18, 9:40-49, 11:10-29, 13:62-15:18, 16:24-37, 18:3-60, 19:1-38.</p> <p>Declaration of Dr. Vijay Madiseti.</p>

EXHIBIT A – Plaintiff’s Terms and Supporting Evidence

<u>No.</u>	<u>Term</u>	<u>Family 6 Asserted Claims</u>	<u>Plaintiff’s Construction and Supporting Evidence</u>
		<p>for reception, a second FIP setting following reception of the flag signal, wherein:</p> <p>the first FIP setting comprises at least one first FIP value, the second FIP setting comprises at least one second FIP value, different than the first FIP value, and the Switching occurs on a pre-defined forward error correction codeword boundary following the flag signal.</p> <p style="text-align: center;"><u>’112 Patent</u></p> <p>8. A transceiver comprising:</p> <p>a receiver operable to receiving, during steady-state communication, using a first forward error correction and interleaving parameter (FIP) setting that comprises a forward error correction (FEC) codeword size and a first number of FEC coding parity bytes; and</p> <p>the receiver further operable to switch, during the steady state communication, to receiving using a second FIP setting that comprises a second FEC codeword size that is different than the first FEC codeword size and a second number of FEC coding parity bytes that is different than the first number of FEC coding parity bytes,</p> <p>wherein the switching to receiving using the second FEC codeword size and the second</p>	

EXHIBIT A – Plaintiff’s Terms and Supporting Evidence

<u>No.</u>	<u>Term</u>	<u>Family 6 Asserted Claims</u>	<u>Plaintiff’s Construction and Supporting Evidence</u>
		number of FEC coding parity bytes is based on a counter reaching a value.	
19.	<p>“FIP setting”</p> <p><u>Family 6:</u> ’835 Patent: Claims 8, 10, 24, 26 ’112 Patent: Claim 8</p>	<p><u>’835 Patent</u></p> <p>8. An apparatus configurable to adapt forward error correction and interleaver parameter (FIP) settings during steady-state communication or initialization comprising: a transceiver, including a processor, configurable to: transmit a signal using a first FIP setting, transmit a flag signal, and switch to using for transmission, a second FIP setting following transmission of the flag signal, wherein: the first FIP setting comprises at least one first FIP value, the second FIP setting comprises at least one second FIP value, different than the first FIP value, and the switching occurs on a pre-defined forward error correction codeword boundary following the flag signal.</p> <p>10. The apparatus of claim 8, wherein a first interleaver parameter value of the first FIP setting is different than a second interleaver parameter value of the second FIP setting.</p>	<p>Plain and ordinary meaning. No construction necessary.</p> <p>’835 Patent Cols. 1:60 – 2:33, 3:37-58, 12:40-64, 13:16-37, 13:43-53; U.S. Prov. Appl. No. 60/549804) at p. 18; ITU-T G.992.3 (7/2002) at § 7.5, § 7.7.1.4, and § 7.7.1.5.</p> <p>Declaration of Dr. Vijay Madiseti.</p>

EXHIBIT A – Plaintiff’s Terms and Supporting Evidence

<u>No.</u>	<u>Term</u>	<u>Family 6 Asserted Claims</u>	<u>Plaintiff’s Construction and Supporting Evidence</u>
		<p>24. An apparatus configurable to adapt forward error correction and interleaver parameter (FIP) settings during steady-state communication or initialization comprising: a transceiver, including a processor, configurable to: receive a signal using a first FIP setting, receive a flag signal, and Switch to using for reception, a second FIP setting following reception of the flag signal, wherein: the first FIP setting comprises at least one first FIP value, the second FIP setting comprises at least one second FIP value, different than the first FIP value, and the Switching occurs on a pre-defined forward error correction codeword boundary following the flag signal.</p> <p>26. The apparatus of claim 24, wherein a first interleaver parameter value of the first FIP setting is different than a second interleaver parameter value of the second FIP setting.</p> <p style="text-align: center;"><u>’112 Patent</u></p> <p>8. A transceiver comprising: a receiver operable to receiving, during steady-state communication, using a first forward error correction and interleaving parameter (FIP) setting that comprises a</p>	

EXHIBIT A – Plaintiff’s Terms and Supporting Evidence

<u>No.</u>	<u>Term</u>	<u>Family 6 Asserted Claims</u>	<u>Plaintiff’s Construction and Supporting Evidence</u>
		<p>forward error correction (FEC) codeword size and a first number of FEC coding parity bytes; and</p> <p>the receiver further operable to switch, during the steady state communication, to receiving using a second FIP setting that comprises a second FEC codeword size that is different than the first FEC codeword size and a second number of FEC coding parity bytes that is different than the first number of FEC coding parity bytes,</p> <p>wherein the switching to receiving using the second FEC codeword size and the second number of FEC coding parity bytes is based on a counter reaching a value.</p>	
20.	<p>“FIP value”</p> <p><u>Family 6:</u> ’835 Patent: Claims 8, 24</p>	<p><u>’835 Patent</u></p> <p>8. An apparatus configurable to adapt forward error correction and interleaver parameter (FIP) settings during steady-state communication or initialization comprising:</p> <p>a transceiver, including a processor, configurable to: transmit a signal using a first FIP setting, transmit a flag signal, and switch to using for transmission, a second FIP setting following transmission of the flag signal,</p> <p>wherein:</p> <p>the first FIP setting comprises at least one first FIP value, the second FIP setting</p>	<p>Plain and ordinary meaning. No construction necessary.</p> <p>’835 Patent, Cols. 1:60-2:33, 3:37-47, 12:40-64, 13:16-37, 13:43-53; U.S. Prov. Appl. No. 60/549804) at p. 18; ITU-T G.992.3 (7/2002) at § 7.5, § 7.7.1.4, and § 7.7.1.5.</p> <p>Declaration of Dr. Vijay Madiseti.</p>

EXHIBIT A – Plaintiff’s Terms and Supporting Evidence

<u>No.</u>	<u>Term</u>	<u>Family 6 Asserted Claims</u>	<u>Plaintiff’s Construction and Supporting Evidence</u>
		<p>comprises at least one second FIP value, different than the first FIP value, and the switching occurs on a pre-defined forward error correction codeword boundary following the flag signal.</p> <p>24. An apparatus configurable to adapt forward error correction and interleaver parameter (FIP) settings during steady-state communication or initialization comprising: a transceiver, including a processor, configurable to: receive a signal using a first FIP setting, receive a flag signal, and Switch to using for reception, a second FIP setting following reception of the flag signal, wherein: the first FIP setting comprises at least one first FIP value, the second FIP setting comprises at least one second FIP value, different than the first FIP value, and the Switching occurs on a pre-defined forward error correction codeword boundary following the flag signal.</p>	
21.	“flag signal” <u>Family 6:</u> ’835 Patent: Claims 8, 24	<u>’835 Patent</u>	“signal used to indicate when an updated FIP setting / interleaver parameter value is to be used (the signal does not contain message data indicating when the updated

EXHIBIT A – Plaintiff’s Terms and Supporting Evidence

<u>No.</u>	<u>Term</u>	<u>Family 6 Asserted Claims</u>	<u>Plaintiff’s Construction and Supporting Evidence</u>
	'162 Patent: Claims 8, 9	<p>8. An apparatus configurable to adapt forward error correction and interleaver parameter (FIP) settings during steady-state communication or initialization comprising:</p> <p>a transceiver, including a processor, configurable to: transmit a signal using a first FIP setting, transmit a flag signal, and switch to using for transmission, a second FIP setting following transmission of the flag signal,</p> <p>wherein:</p> <p>the first FIP setting comprises at least one first FIP value, the second FIP setting comprises at least one second FIP value, different than the first FIP value, and the switching occurs on a pre-defined forward error correction codeword boundary following the flag signal.</p> <p>24. An apparatus configurable to adapt forward error correction and interleaver parameter (FIP) settings during steady-state communication or initialization comprising:</p> <p>a transceiver, including a processor, configurable to:</p> <p>receive a signal using a first FIP setting, receive a flag signal, and Switch to using for reception, a second FIP setting following reception of the flag signal,</p> <p>wherein:</p>	<p>FIP setting / interleaver parameter value is to be used)”</p> <p>'835 patent, Fig. 6, Cols. 11:4-9, 11:66-12:37, 19:15-22.</p> <p>ITU-T G.992.3 (7/2002) at § 8.7.3.</p> <p>Declaration of Dr. Vijay Madiseti.</p>

EXHIBIT A – Plaintiff’s Terms and Supporting Evidence

<u>No.</u>	<u>Term</u>	<u>Family 6 Asserted Claims</u>	<u>Plaintiff’s Construction and Supporting Evidence</u>
		<p>the first FIP setting comprises at least one first FIP value, the second FIP setting comprises at least one second FIP value, different than the first FIP value, and the Switching occurs on a pre-defined forward error correction codeword boundary following the flag signal.</p> <p style="text-align: center;"><u>’162 Patent</u></p> <p>8. A device comprising: an interleaver configured to interleave a plurality of bits: and a transmitter portion coupled to the interleaver and configured to: transmit using a first interleaver parameter value; transmit a flag signal; and change to transmitting using a second interleaver parameter value that is different than the first interleaver parameter value, wherein the second interleaver parameter value is used for transmission on a pre-defined forward error correction codeword boundary following transmission of the flag signal.</p> <p>9. The device of claim 8, wherein the flag signal is an inverted Sync symbol.</p>	

EXHIBIT A – Plaintiff’s Terms and Supporting Evidence

<u>No.</u>	<u>Term</u>	<u>Family 6 Asserted Claims</u>	<u>Plaintiff’s Construction and Supporting Evidence</u>
22.	<p>“interleaver parameter value”</p> <p><u>Family 6:</u> ’835 Patent: Claims 10, 26</p> <p>’162 Patent: Claim 8</p>	<p><u>’835 Patent</u></p> <p>10. The apparatus of claim 8, wherein a first interleaver parameter value of the first FIP setting is different than a second interleaver parameter value of the second FIP setting.</p> <p>26. The apparatus of claim 24, wherein a first interleaver parameter value of the first FIP setting is different than a second interleaver parameter value of the second FIP setting.</p> <p><u>’162 Patent</u></p> <p>8. A device comprising: an interleaver configured to interleave a plurality of bits: and a transmitter portion coupled to the interleaver and configured to: transmit using a first interleaver parameter value; transmit a flag signal; and change to transmitting using a second interleaver parameter value that is different than the first interleaver parameter value, wherein the second interleaver parameter value is used for transmission on a pre-defined forward error correction codeword</p>	<p>Plain and ordinary meaning. No construction necessary.</p> <p>’835 Patent, Cols. 1:60 – 2:33, 2:44-49, 3:37-58, 12:40-64, 13:16-37, 13:43-53; U.S. Prov. Appl. No. 60/549804) at p. 18; (ITU-T G.992.3 (7/2002) at § 7.5, § 7.7.1.4, and § 7.7.1.5.</p> <p>Declaration of Dr. Vijay Madiseti.</p>

EXHIBIT A – Plaintiff’s Terms and Supporting Evidence

<u>No.</u>	<u>Term</u>	<u>Family 6 Asserted Claims</u>	<u>Plaintiff’s Construction and Supporting Evidence</u>
		boundary following transmission of the flag signal.	

EXHIBIT A – Plaintiff’s Terms and Supporting Evidence**VIII. FAMILY 9**

<u>No.</u>	<u>Term</u>	<u>Family 9 Asserted Claims</u>	<u>Plaintiff’s Construction and Supporting Evidence</u>
23.	<p>“higher immunity to noise”</p> <p><u>Family 9:</u></p> <p>’348 Patent: Claims 2 and 10</p> <p>’809 Patent: Claims 2, 9, 16, 23</p>	<p><u>’348 Patent</u></p> <p>2. The apparatus of claim 1, wherein the received messages have a higher immunity to noise than the transmitted packet.</p> <p>10. The apparatus of claim 9, wherein the transmitted messages have a higher immunity to noise than the received packet.</p> <p><u>’809 Patent</u></p> <p>2. The apparatus of claim 1, wherein the received message has a higher immunity to noise than the transmitted packet.</p> <p>9. The apparatus of claim 8, wherein the transmitted message has a higher immunity to noise than the received packet.</p> <p>16. The media of claim 15, wherein the received message has a higher immunity to noise than the transmitted packet.</p> <p>23. The media of claim 22, wherein the transmitted message has a higher immunity to noise than the received packet.</p>	<p>“higher SNR margin”</p> <p>’348 Patent, Col. 16:4-9</p> <p>’956 Patent at 1:65-66</p> <p>’956 Patent) at 17:47-48</p> <p>’956 Patent at 18:5</p>

EXHIBIT A – Plaintiff’s Terms and Supporting Evidence

<u>No.</u>	<u>Term</u>	<u>Family 9 Asserted Claims</u>	<u>Plaintiff’s Construction and Supporting Evidence</u>
24.	<p>“PTM-TC [(Packet Transfer Mode Transmission Convergence)] codewords”</p> <p><u>Family 9:</u> ’577 Patent: Claims 16, 37 ’348 Patent: Claims 1, 9 ’055 Patent: Claim 17</p>	<p><u>’577 Patent</u></p> <p>16. An apparatus comprising: a multicarrier transceiver operable to receive at least one packet using deinterleaving, and transmit at least one message without using interleaving, wherein the at least one message includes information that indicates an acknowledgement (ACK) or a negative acknowledgement (NACK) of the at least one packet, wherein the at least one packet comprises one or more PTM-TC codewords.</p> <p>37. An apparatus comprising: a multicarrier transceiver operable to transmit at least one packet using interleaving, and receive at least one message without using interleaving, wherein the at least one message includes information that indicates an acknowledgement (ACK) or a negative acknowledgement (NACK) of the at least one packet, wherein the at least one packet comprises one or more PTM-TC code words.</p> <p><u>’348 Patent</u></p> <p>1. An apparatus comprising: a multicarrier transceiver including a processor and memory operable to:</p>	<p>Plain and ordinary meaning. No construction necessary.</p> <p>’348 Patent, Cols. 2:24-29, 2:55-59, 3:9-12, 4:12-16, 10:3-48.</p>

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<u>No.</u>	<u>Term</u>	<u>Family 9 Asserted Claims</u>	<u>Plaintiff’s Construction and Supporting Evidence</u>
		<p>transmit a packet using a forward error correction encoder and an interleaver, wherein the packet comprises a header field and a plurality of PTM-TC codewords, a plurality of ATM cells or a plurality of Reed-Solomon codewords, and wherein the header field comprises a sequence identifier (SID); and</p> <p>receive a plurality of messages using a forward error correction decoder and without using a deinterleaver, wherein each message of the plurality of messages is received in a different DMT symbol and wherein at least one message of the plurality of messages includes an acknowledgement (ACK) or a negative acknowledgement (NACK) of the transmitted packet.</p> <p>9. An apparatus comprising: a multicarrier transceiver including a processor and memory operable to: receive a packet using a forward error correction decoder and a deinterleaver, wherein the packet comprises a header field and a plurality of PTM-TC codewords, a plurality of ATM cells or a plurality of Reed-Solomon codewords, and wherein the header field comprises a sequence identifier (SID); and</p>	

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		<p>transmit a plurality of messages using a forward error correction encoder and without using an interleaver, wherein each message of the plurality of messages is transmitted in a different DMT symbol and wherein at least one message of the plurality of messages includes an acknowledgement (ACK) or a negative acknowledgement (NACK) of the received packet.</p> <p><u>’055 Patent</u></p> <p>17. The transceiver of claim 11, wherein the first type of packet comprises one or more PTM-TC (Packet Transfer Mode-Transmission Convergence) codewords.</p>	
25.	<p>“receive at least one packet using deinterleaving”</p> <p><u>Family 9:</u> ’577 Patent: Claims 16, 30</p>	<p><u>’557 Patent</u></p> <p>16. An apparatus comprising: a multicarrier transceiver operable to receive at least one packet using deinterleaving, and transmit at least one message without using interleaving, wherein the at least one message includes information that indicates an acknowledgement (ACK) or a negative acknowledgement (NACK) of the at least one packet, wherein the at least one packet comprises one or more PTM-TC codewords.</p> <p>30. An apparatus comprising:</p>	<p>Plain and ordinary meaning. No construction necessary.</p> <p>’348 Patent, Fig. 1, Fig. 3, Cols. 19:43—20:17, 21:4-29</p>

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<u>No.</u>	<u>Term</u>	<u>Family 9 Asserted Claims</u>	<u>Plaintiff’s Construction and Supporting Evidence</u>
		a multicarrier transceiver operable to receive at least one packet using deinterleaving , and transmit at least one message without using interleaving, wherein the at least one message includes information that indicates an acknowledgement (ACK) or a negative acknowledgement (NACK) of the at least one packet, wherein the at least one packet comprises one or more Reed-Solomon code-words.	
26.	<p>“[transmit/retransmit] at least one packet using interleaving”</p> <p><u>Family 9:</u> ’577 Patent: Claims 37, 38, 53, 54</p>	<p><u>’557 Patent</u></p> <p>37. An apparatus comprising: a multicarrier transceiver operable to transmit at least one packet using interleaving, and receive at least one message without using interleaving, wherein the at least one message includes information that indicates an acknowledgement (ACK) or a negative acknowledgement (NACK) of the at least one packet, wherein the at least one packet comprises one or more PTM-TC code-words.</p> <p>38. The apparatus of claim 37, wherein the transceiver is operable to retransmit at least one packet using interleaving.</p> <p>53. An apparatus comprising:</p>	<p>Plain and ordinary meaning. No construction necessary.</p> <p>’348 Patent, Fig. 1, Fig. 3, Cols. 2:35-42, 19:43—20:17, 21:4-29</p>

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<u>No.</u>	<u>Term</u>	<u>Family 9 Asserted Claims</u>	<u>Plaintiff’s Construction and Supporting Evidence</u>
		<p>a multicarrier transceiver operable to transmit at least one packet using interleaving, and receive at least one message without using interleaving, wherein the at least one message includes information that indicates an acknowledgement (ACK) or a negative acknowledgement (NACK) of the at least one packet, wherein the at least one packet comprises one or more Reed-Solomon code words.</p> <p>54. The apparatus of claim 53, wherein the transceiver is operable to retransmit at least one packet using interleaving.</p>	
27.	<p>“[transmit/receive] a [packet/plurality of messages] using a forward error correction [encoder/decoder] and [without using] [an/a interleaver/deinterleaver]”</p> <p><u>Family 9:</u> '348 Patent: Claims 1, 9</p>	<p><u>'348 Patent</u></p> <p>1. An apparatus comprising: a multicarrier transceiver including a processor and memory operable to: transmit a packet using a forward error correction encoder and an interleaver, wherein the packet comprises a header field and a plurality of PTM-TC codewords, a plurality of ATM cells or a plurality of Reed-Solomon codewords, and wherein the header field comprises a sequence identifier (SID); and receive a plurality of messages using a forward error correction decoder and without using a deinterleaver, wherein each</p>	<p>Plain and ordinary meaning. No construction necessary.</p> <p>'348 Patent, Cols. 15:14-29, 19:43-20:17.</p>

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<u>No.</u>	<u>Term</u>	<u>Family 9 Asserted Claims</u>	<u>Plaintiff’s Construction and Supporting Evidence</u>
		<p>message of the plurality of messages is received in a different DMT symbol and wherein at least one message of the plurality of messages includes an acknowledgement (ACK) or a negative acknowledgement (NACK) of the transmitted packet.</p> <p>9. An apparatus comprising: a multicarrier transceiver including a processor and memory operable to: receive a packet using a forward error correction decoder and a deinterleaver, wherein the packet comprises a header field and a plurality of PTM-TC codewords, a plurality of ATM cells or a plurality of Reed-Solomon codewords, and wherein the header field comprises a sequence identifier (SID); and transmit a plurality of messages using a forward error correction encoder and without using an interleaver, wherein each message of the plurality of messages is transmitted in a different DMT symbol and wherein at least one message of the plurality of messages includes an acknowledgement (ACK) or a negative acknowledgement (NACK) of the received packet.</p>	

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<u>No.</u>	<u>Term</u>	<u>Family 9 Asserted Claims</u>	<u>Plaintiff’s Construction and Supporting Evidence</u>
28.	<p>“transmitting, by the transceiver, a packet using a forward error correction encoder and an interleaver”</p> <p><u>Family 9:</u> ’4473 Patent: Claim 1</p>	<p><u>’4437 Patent</u></p> <p>1. An apparatus comprising: a multicarrier transceiver including a processor and memory operable to reduce a packet error rate by: transmitting, by the transceiver, a packet using a forward error correction encoder and an interleaver, wherein the packet comprises a header field and a plurality of bytes, and wherein the header field comprises a sequence identifier (SID); and receiving, by the transceiver, at least one message using a forward error correction decoder and without using a deinterleaver, wherein the at least one message is received in a single discrete multitone (DMT) symbol and wherein the at least one message includes an acknowledgement (ACK) or a negative acknowledgement (NACK) of the transmitted packet, wherein an SNR margin of the at least one message is greater than an SNR margin of the packet; and reducing the packet error rate by retransmitting, by the transceiver and when there is the negative acknowledgement (NACK) in the at least one message, the packet.</p>	<p>Plain and ordinary meaning. No construction necessary.</p> <p>’348 Patent, Fig. 1, Fig. 3, Cols. 2:35-42, 19:43-20:17, 21:4-29</p>

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<u>No.</u>	<u>Term</u>	<u>Family 9 Asserted Claims</u>	<u>Plaintiff’s Construction and Supporting Evidence</u>
29.	<p>“receiving, by the transceiver, at least one message using a forward error correction decoder and without using a deinterleaver”</p> <p><u>Family 9:</u> ‘4473 Patent: Claim 1</p>	<p><u>’4437 Patent</u></p> <p>1. An apparatus comprising: a multicarrier transceiver including a processor and memory operable to reduce a packet error rate by: transmitting, by the transceiver, a packet using a forward error correction encoder and an interleaver, wherein the packet comprises a header field and a plurality of bytes, and wherein the header field comprises a sequence identifier (SID); and receiving, by the transceiver, at least one message using a forward error correction decoder and without using a deinterleaver, wherein the at least one message is received in a single discrete multi-tone (DMT) symbol and wherein the at least one message includes an acknowledgement (ACK) or a negative acknowledgement (NACK) of the transmitted packet, wherein an SNR margin of the at least one message is greater than an SNR margin of the packet; and reducing the packet error rate by retransmitting, by the transceiver and when there is the negative acknowledgement (NACK) in the at least one message, the packet.</p>	<p>Plain and ordinary meaning. No construction necessary.</p> <p>’348 Patent, Cols. 15:14-29, 19:43-20:17.</p>

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<u>No.</u>	<u>Term</u>	<u>Family 9 Asserted Claims</u>	<u>Plaintiff’s Construction and Supporting Evidence</u>
30.	<p>“[transmitting/transmit/receiving/receive] a [packet/message] using forward error correction [encoding/decoding] and [without using] [interleaving/deinterleaving]”</p> <p><u>Family 9:</u> '809 Patent: Claims 1, 8, 15, 22</p>	<p><u>'809 Patent</u></p> <p>1. An apparatus comprising: a multicarrier transceiver including a processor and memory capable of: transmitting a packet using forward error correction encoding and interleaving, wherein the packet comprises a header field and a plurality of Reed-Solomon code words, and wherein the header field comprises a sequence identifier (SID); and receiving a message using forward error correction decoding and without using deinterleaving, wherein the message is received in a single DMT symbol, and wherein the message includes an acknowledgement (ACK) or a negative acknowledgement (NACK) of the transmitted packet.</p> <p>8. An apparatus comprising: a multicarrier transceiver including a processor and memory capable of: receiving a packet using forward error correction decoding and deinterleaving, wherein the packet comprises a header field and a plurality of Reed-Solomon code words, and wherein the header field comprises a sequence identifier (SID); and transmitting a message using forward error correction encoding and without us-</p>	<p>Plain and ordinary meaning. No construction necessary.</p> <p>'348 Patent, Fig. 1, Fig. 3, Cols. 2:35-42, 15:14-29, 19:43-20:17, 21:4-29</p>

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<u>No.</u>	<u>Term</u>	<u>Family 9 Asserted Claims</u>	<u>Plaintiff’s Construction and Supporting Evidence</u>
		<p>ing interleaving, wherein the message is transmitted in a single DMT symbol and wherein the message includes an acknowledgement (ACK) or a negative acknowledgement (NACK) of the received packet.</p> <p>15. A non-transitory computer-readable information storage media having stored thereon instructions, that when executed by one or more processors in a transceiver, cause the transceiver to:</p> <p>transmit a packet using forward error correction encoding and interleaving, wherein the packet comprises a header field and a plurality of Reed-Solomon codewords, and wherein the header field comprises a sequence identifier (SID); and</p> <p>receive a message using forward error correction decoding and without using deinterleaving, wherein the message is received in a single DMT symbol, and wherein the message includes an acknowledgement (ACK) or a negative acknowledgement (NACK) of the transmitted packet.</p> <p>22. A non-transitory computer-readable information storage media having stored thereon instructions, that when executed by</p>	

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<u>No.</u>	<u>Term</u>	<u>Family 9 Asserted Claims</u>	<u>Plaintiff’s Construction and Supporting Evidence</u>
		<p>one or more processors in a transceiver, cause the transceiver to:</p> <p>receive a packet using forward error correction decoding and deinterleaving, wherein the packet comprises a header field and a plurality of Reed-Solomon codewords, and wherein the header field comprises a sequence identifier (SID); and</p> <p>transmit a message using forward error correction encoding and without using interleaving, wherein the message is transmitted in a single DMT symbol and wherein the message includes an acknowledgement (ACK) or a negative acknowledgement (NACK) of the received packet</p>	
31.	<p>“[retransmit/retransmitting] the packet using [the] forward error correction [encoder/encoding] and [the interleaver/interleaving]”</p> <p><u>Family 9:</u> ’348 Patent: Claim 3 ’4473 Patent: Claim 3 ’809 Patent: Claims 3, 17</p>	<p><u>’348 Patent</u></p> <p>3. The apparatus of claim 1, wherein the transceiver is operable to retransmit the packet using the forward error correction encoder and the interleaver.</p> <p><u>’4473 Patent</u></p> <p>3. The apparatus of claim 1, wherein the transceiver is operable to retransmit the packet using the forward error correction encoder and the interleaver.</p> <p><u>’809 Patent</u></p>	<p>Plain and ordinary meaning. No construction necessary.</p> <p>’348 Patent, Fig. 1, Fig. 3, Cols. 2:35-42, 19:43-20:17, 21:4-29</p>

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<u>No.</u>	<u>Term</u>	<u>Family 9 Asserted Claims</u>	<u>Plaintiff’s Construction and Supporting Evidence</u>
		<p>3. The apparatus of claim 1, wherein the transceiver is capable of retransmitting the packet using forward error correction encoding and interleaving.</p> <p>17. The media of claim 15, wherein instructions further cause the transceiver to retransmit the packet using forward error correction encoding and interleaving.</p>	
32.	<p>“[receive/receiving] a re-transmitted packet using [the] forward error correction [decoder/decoding] and [the deinterleaver/deinterleaving]”</p> <p><u>Family 9:</u> ‘348 Patent: Claim 11 ‘809 Patent: Claim 10</p>	<p><u>‘348 Patent</u></p> <p>11. The apparatus of claim 9, wherein the transceiver is operable to receive a retransmitted packet using the forward error correction decoder and the deinterleaver.</p> <p><u>‘809 Patent</u></p> <p>10. The apparatus of claim 8, wherein the transceiver is capable of receiving a retransmitted packet using forward error correction decoding and deinterleaving.</p>	Plain and ordinary meaning. No construction necessary.

EXHIBIT A – Plaintiff’s Terms and Supporting Evidence**IX. FAMILY 10**

<u>No.</u>	<u>Term</u>	<u>Family 10 Asserted Claims</u>	<u>Plaintiff’s Construction and Supporting Evidence</u>
33.	<p>“A multicarrier communications transceiver operable to: receive a multicarrier symbol comprising a first plurality of carriers”</p> <p><u>Family 10:</u> '354 Patent: Claim 10</p>	<p><u>'354 Patent</u></p> <p>10. A multicarrier communications transceiver operable to: receive a multicarrier symbol comprising a first plurality of carriers and a second plurality of carriers; receive a first plurality of bits on the first plurality of carriers using a first SNR margin; receive a second plurality of bits on the second plurality of carriers using a second SNR margin; wherein the first plurality of carriers is different than the second plurality of carriers, wherein the first SNR margin is different than the second SNR margin, and wherein the first SNR margin provides more robust than the second SNR margin.</p>	<p>Plain and ordinary meaning. No construction necessary.</p> <p>'354 Patent Cols. 1:27-2:3, 3:26-67, 4:65-5:36.</p>
34.	<p>“receive a first plurality of bits on the first plurality of carriers using a first SNR margin; receive a second plurality of bits on the second plurality of carriers using a second SNR margin”</p>	<p><u>'354 Patent</u></p> <p>10. A multicarrier communications transceiver operable to: receive a multicarrier symbol comprising a first plurality of carriers and a second plurality of carriers;</p>	<p>Plain and ordinary meaning. No construction necessary.</p> <p>'354 Patent Cols. Fig. 2, 1:27—2:40, 3:26-67, 4:65-5:36, 7:56-8:37.</p>

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<u>No.</u>	<u>Term</u>	<u>Family 10 Asserted Claims</u>	<u>Plaintiff’s Construction and Supporting Evidence</u>
	<u>Family 10:</u> ’354 Patent: Claim 10	receive a first plurality of bits on the first plurality of carriers using a first SNR margin; receive a second plurality of bits on the second plurality of carriers using a second SNR margin; wherein the first plurality of carriers is different than the second plurality of carriers, wherein the first SNR margin is different than the second SNR margin, and wherein the first SNR margin provides more robust than the second SNR margin.	
35.	“wherein the first SNR margin provides more robust reception than the second SNR margin” <u>Family 10:</u> ’354 Patent: Claim 10	<u>’354 Patent</u> 10. A multicarrier communications transceiver operable to: receive a multicarrier symbol comprising a first plurality of carriers and a second plurality of carriers; receive a first plurality of bits on the first plurality of carriers using a first SNR margin; receive a second plurality of bits on the second plurality of carriers using a second SNR margin; wherein the first plurality of carriers is different than the second plurality of carriers, wherein the first SNR margin is different than the second SNR margin, and	Plain and ordinary meaning. No construction necessary. ’354 Patent Cols. 2:4-40, 3:27-67, 4:65-5:36; 6:65-7:18; 5:25-6:3; 7:3-42

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<u>No.</u>	<u>Term</u>	<u>Family 10 Asserted Claims</u>	<u>Plaintiff’s Construction and Supporting Evidence</u>
		wherein the first SNR margin provides more robust than the second SNR margin.	
36.	<p>“signal to noise ratio (SNR) margin” / “SNR margin”</p> <p><u>Family 10:</u> ’988 Patent: Claim 16 ’354 Patent: Claims 10, 11, 12</p>	<p><u>’988 Patent:</u> 16. An apparatus comprising: a multicarrier communications transceiver operable to demodulate for reception a first plurality of bits from a first carrier using a first Signal to Noise Ratio (SNR) margin and to demodulate for reception a second plurality of bits from a second carrier using a second SNR margin, and to demodulate for reception a third plurality of bits from the first carrier using a third SNR margin, wherein the first SNR margin specifies a first value for an allowable increase in noise without an increase in the bit error rate (BER) associated with the first carrier, wherein the second SNR margin specifies a second value for an allowable increase in noise without an increase in the bit error rate (BER) associated with the second carrier, wherein the third SNR margin specifies a third value for an allowable increase in noise without an increase in the bit error</p>	<p>Plain and ordinary meaning. No construction necessary.</p> <p>’988 Patent Cols 2:1-25.</p> <p>’354 Patent Cols. 2:4-40.</p>

EXHIBIT A – Plaintiff’s Terms and Supporting Evidence

<u>No.</u>	<u>Term</u>	<u>Family 10 Asserted Claims</u>	<u>Plaintiff’s Construction and Supporting Evidence</u>
		<p>rate (BER) associated with said first carrier, wherein the first SNR margin is different than the second SNR margin, wherein the first SNR margin is different than the third SNR margin, and wherein the first plurality of bits, the second plurality of bits and the third plurality of bits are each different from one another.</p> <p><u>’354 Patent:</u></p> <p>10. A multicarrier communications transceiver operable to: receive a multicarrier symbol comprising a first plurality of carriers and a second plurality of carriers; receive a first plurality of bits on the first plurality of carriers using a first SNR margin; receive a second plurality of bits on the second plurality of carriers using a second SNR margin; wherein the first plurality of carriers is different than the second plurality of carriers, wherein the first SNR margin is different than the second SNR margin, and wherein the first SNR margin provides more robust [transmission than the second SNR margin.]</p>	

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<u>No.</u>	<u>Term</u>	<u>Family 10 Asserted Claims</u>	<u>Plaintiff’s Construction and Supporting Evidence</u>
		<p>11. The transceiver of claim 10, wherein the first SNR margin specifies a first value for an increase in noise associated with the first plurality of carriers.</p> <p>12. The transceiver of claim 10, wherein the second SNR margin specifies a second value for an increase in noise associated with the second plurality of carriers.</p>	